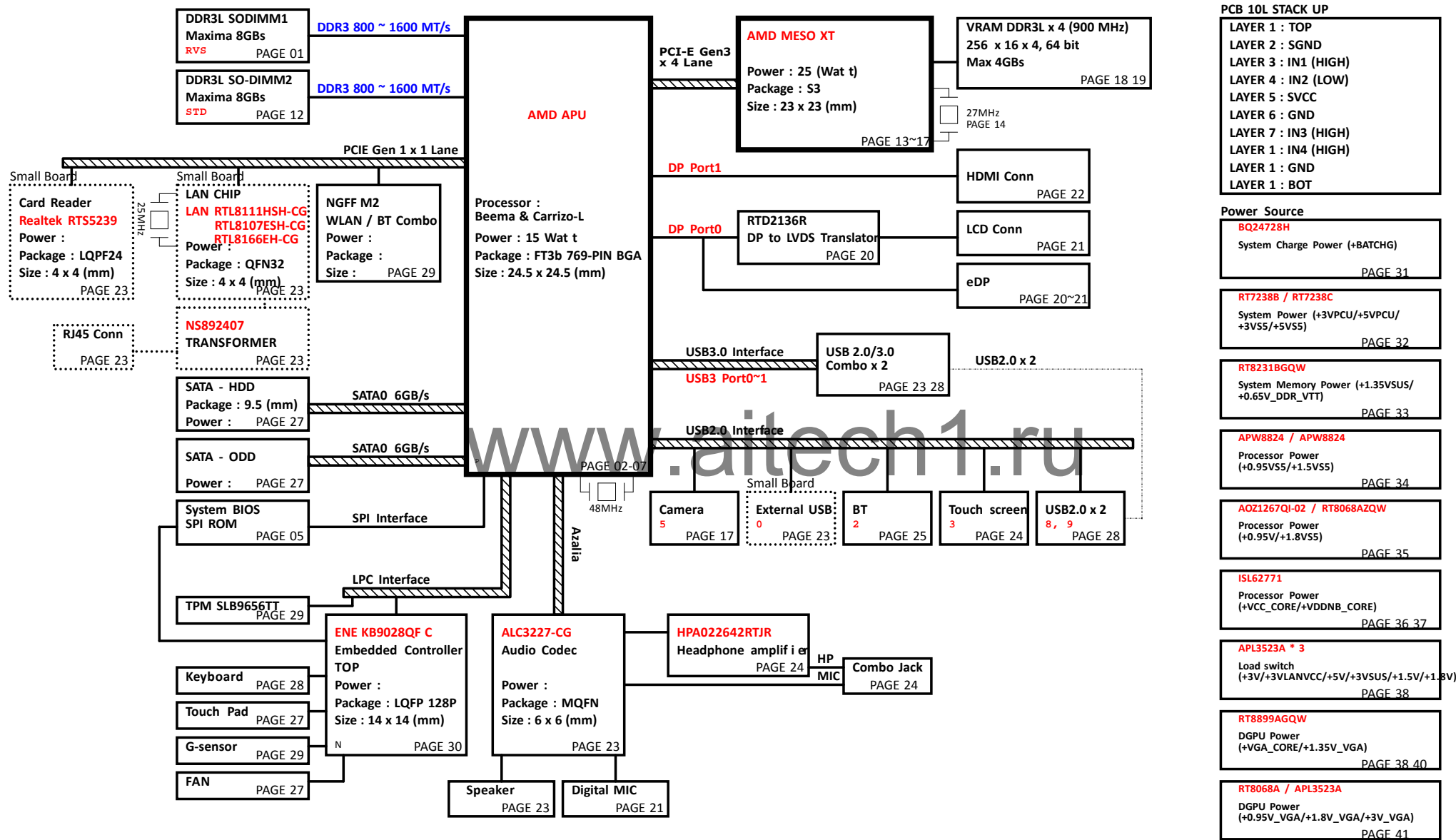
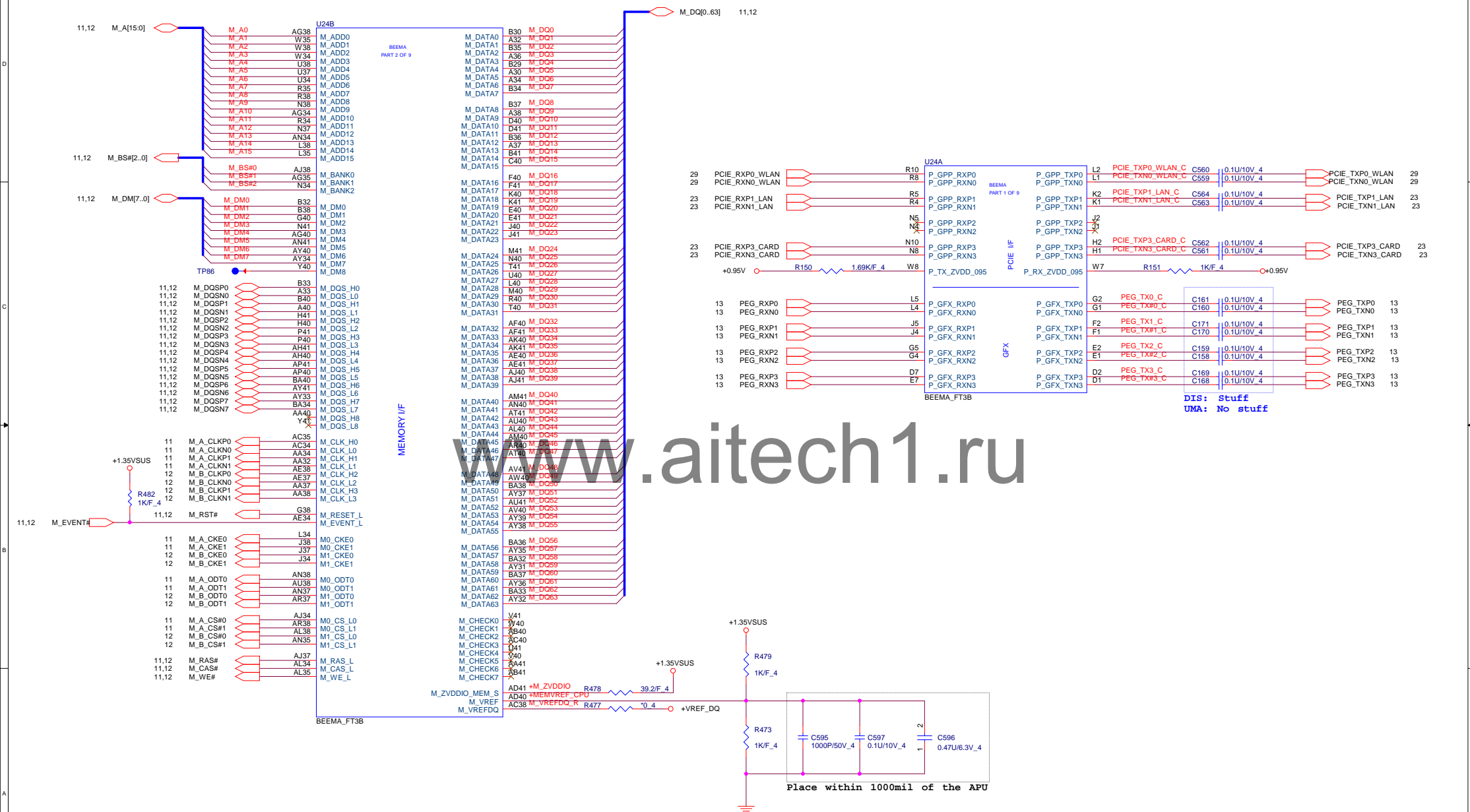
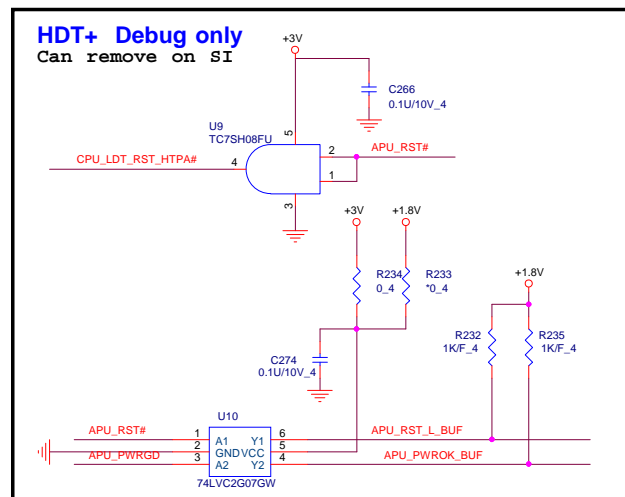


Chocolate AMD Beema DIS/UMA (14.0"/15.6"/17.3")







MV co-layout Kabini

APU_RST# R539 *0.4 APU_TEMPIN1
APU_PWRGD R540 *0.4 APU_TEMPIN2

APU_SIC B22
APU_SID B21

APU_TEMPIN0 A29
APU_TEMPIN1 A20
APU_TEMPIN2 A19

APU_TEMPINRETURN A23

APU_RST# B20
APU_PWRGD B19
APU_PROCHOT# A22
APU_ALERT# B18

APU_TDI D29
APU_TCK D31
APU_TMS D35
APU_TRST# G27
APU_DBRDY B25
APU_DBREQ# A25

VDDCR_NB_SENSE A23
VDDCR_CPU_SENSE E25
VDDCR_MEM_S_SENSE E23
VSS_SENSE E23

VDD_095_FB_H AV33
VDD_095_FB_L AV33

VDDCR_NB_SENSE TP48
VDDCR_CPU_SENSE TP36

TP87
TP83
TP81

TP82
TP80
TP81

TP7003
TP43
TP84

TP42

TP42

TP42

TP42

TP42

TP42

TP42

TP42

TP42

TP42

TP42

TP42

Place near connector

IN_D2 C262 0.1U/10V_4
IN_D2# C256 0.1U/10V_4

IN_D1 C250 0.1U/10V_4
IN_D1# C242 0.1U/10V_4

IN_D0 C258 0.1U/10V_4
IN_D0# C255 0.1U/10V_4

IN_CLK C243 0.1U/10V_4
IN_CLK# C239 0.1U/10V_4

INT_eDP_TXP0 A4
INT_eDP_TXN0 B4

INT_eDP_TXP1 A5
INT_eDP_TXN1 B5

INT_eDP_TXP2 A6
INT_eDP_TXN2 B6

INT_eDP_TXP3 A7
INT_eDP_TXN3 B7

CLK_APU_P K15
CLK_APU_N H15

SVT G31
SVC D27
SVD E29

APU_SIC B22
APU_SID B21

APU_TEMPIN0 A29
APU_TEMPIN1 A20
APU_TEMPIN2 A19

APU_TEMPINRETURN A23

APU_RST# B20
APU_PWRGD B19
APU_PROCHOT# A22
APU_ALERT# B18

APU_TDI D29
APU_TCK D31
APU_TMS D35
APU_TRST# G27
APU_DBRDY B25
APU_DBREQ# A25

VDDCR_NB_SENSE A23
VDDCR_CPU_SENSE E25
VDDCR_MEM_S_SENSE E23
VSS_SENSE E23

VDD_095_FB_H AV33
VDD_095_FB_L AV33

VDDCR_NB_SENSE TP48
VDDCR_CPU_SENSE TP36

TP87
TP83
TP81

TP82
TP80
TP81

TP7003
TP43
TP84

TP42

TP42

TP42

TP42

TP42

TP42

TP42

TP42

TP42

TP42

TP42

IO Thermal Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Serial VID

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

Close to thermal fin

VFIX MODE VID Override table (VDD)

SVC	SVD	Boot Voltage
-----	-----	--------------

0	0	1.1V
---	---	------

0	1	1.0V
---	---	------

1	0	0.9V
---	---	------

1	1	0.8V
---	---	------

1	1	0.8V
---	---	------

1	1	0.8V
---	---	------

1	1	0.8V
---	---	------

1	1	0.8V
---	---	------

1	1	0.8V
---	---	------

1	1	0.8V
---	---	------

1	1	0.8V
---	---	------

1	1	0.8V
---	---	------

HDT+ Connector for Debug only

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

close to HDT debug HEADER

Thermal Sensor

close to thermal fin

close to thermal fin

close to thermal fin

close to thermal fin

close to thermal fin

close to thermal fin

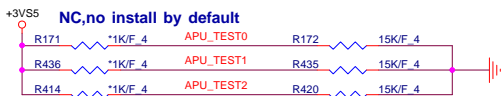
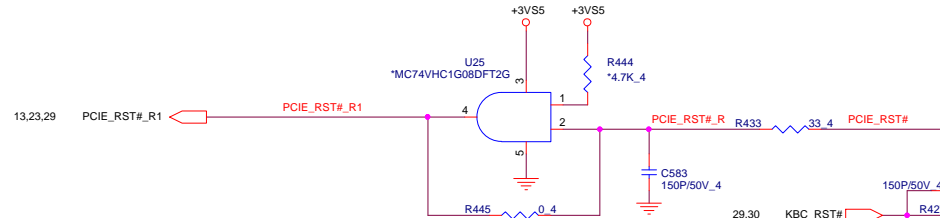
close to thermal fin

PROJECT : Y2x
Quanta Computer Inc.

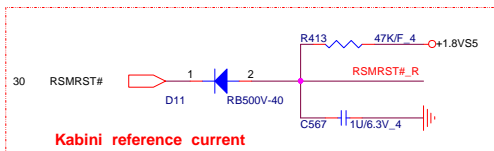
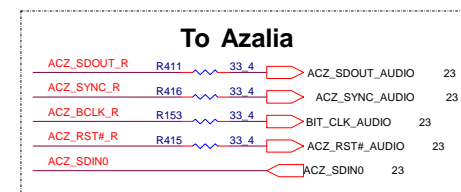
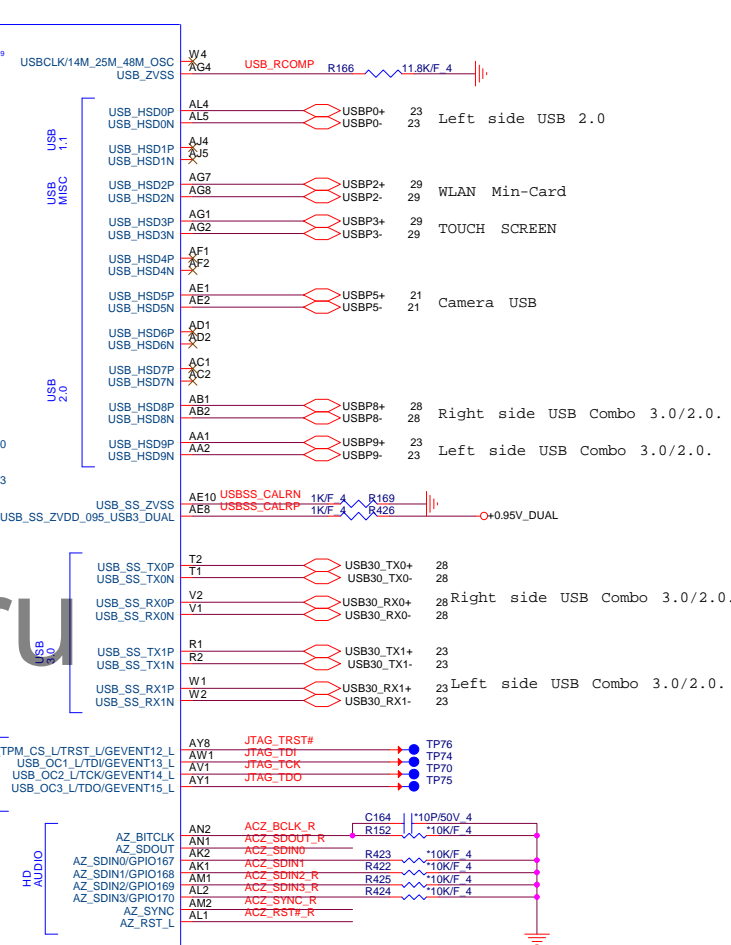
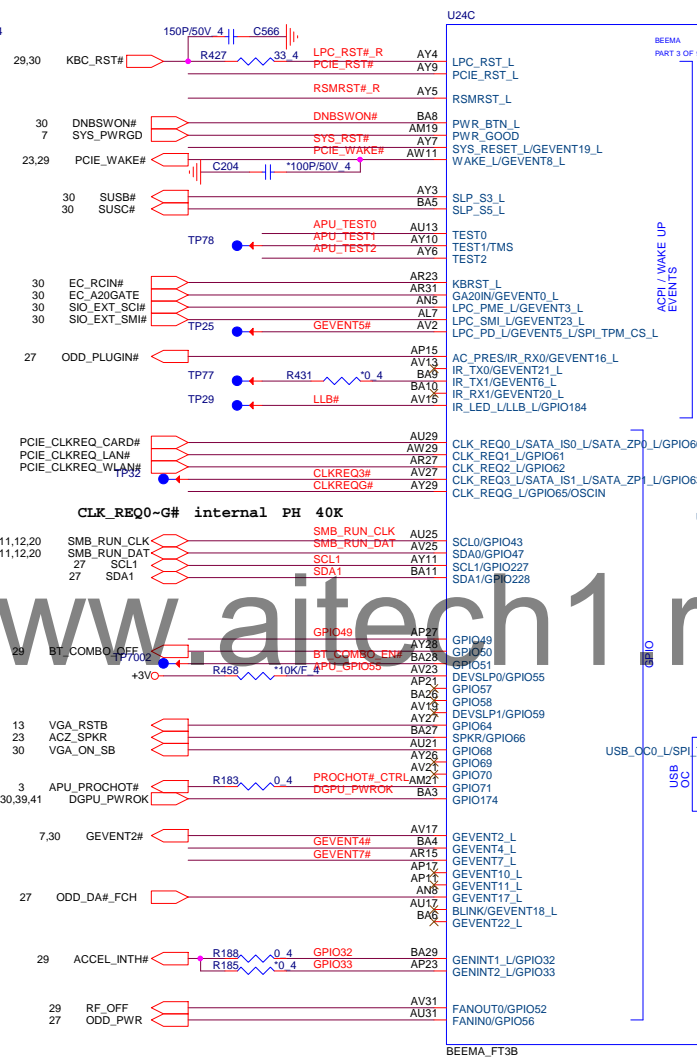
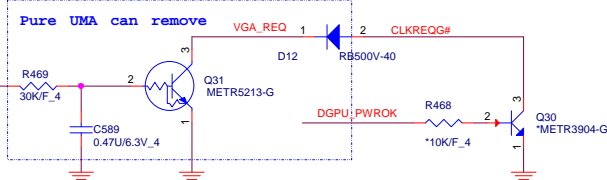
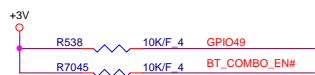
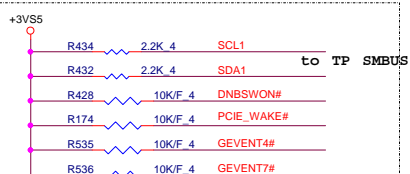
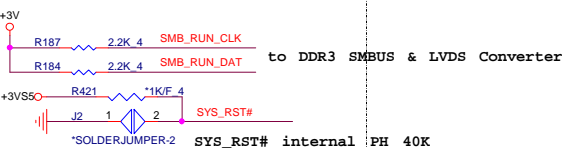
Size Document Number
DIS/MI (2/6)

Rev 1A

Date: Tuesday, November 18, 2014 | Sheet 3 of 41



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted. FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



BOARD ID SETTING

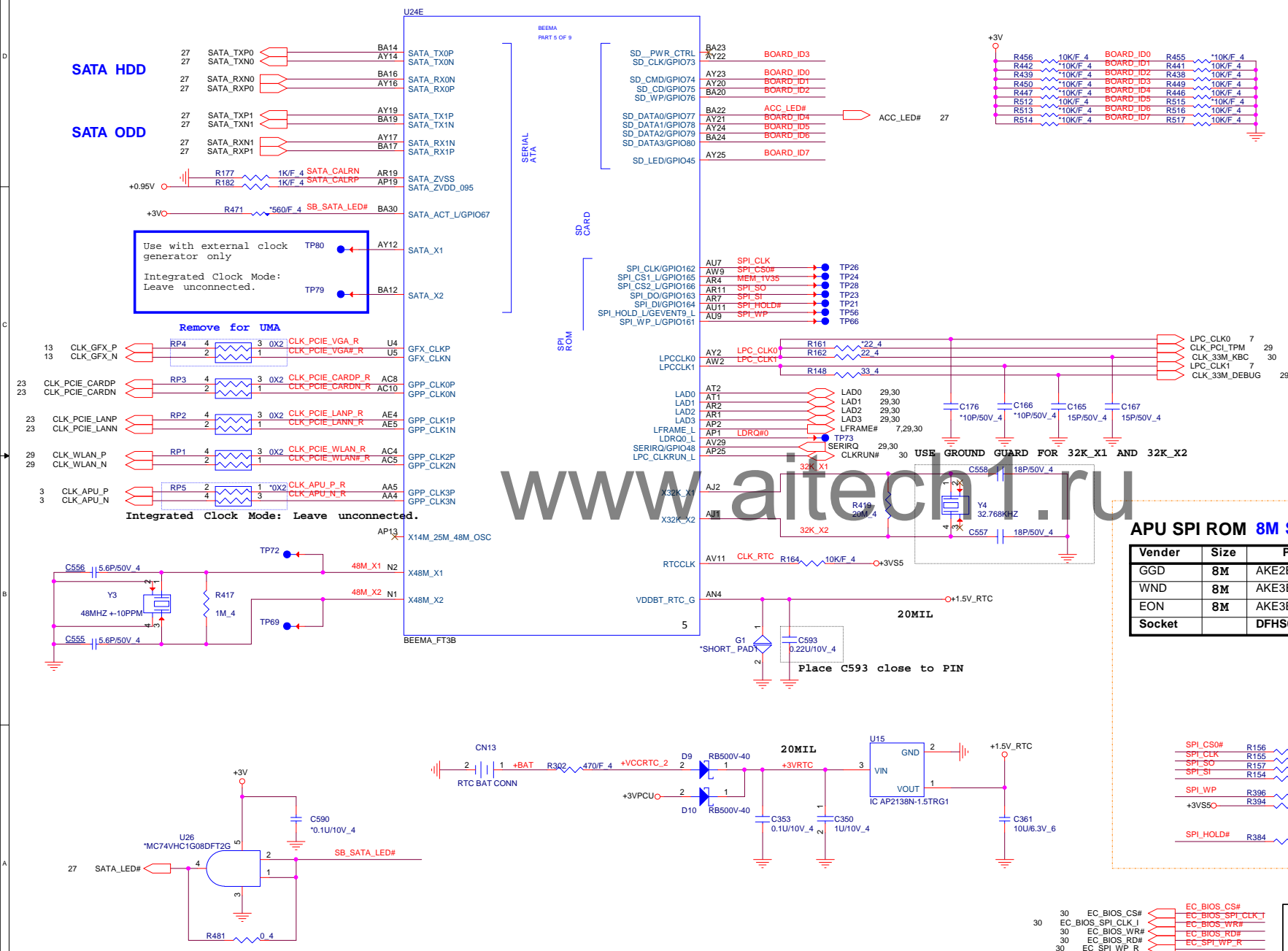
Board ID [0]	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14"
01	15"
10	17"

Board ID [4:3]	Definition
00	Pavilion
01	Reserve
10	Reserve

Board ID [5]	Definition
0	Beema
1	Carrizo-L

Board ID [7:6]	Definition
000	Reserve



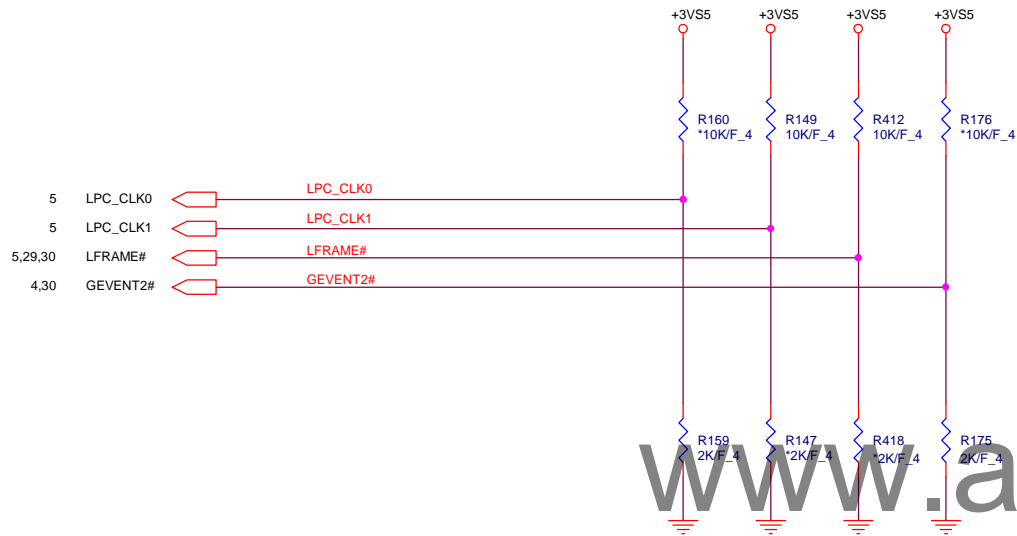
PROJECT : Y2x
Quanta Computer Inc.

Size	Document Number	Rev
	SATA/CLK (4/6)	1A
Date: Tuesday, November 18, 2014	Sheet 5 of 41	

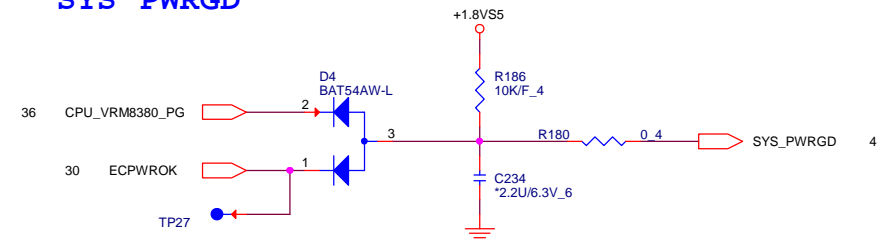


STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



SYS_PWRGD



REQUIRED STRAPS

	LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH	BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT



NB5/RD3

PROJECT : Y2x
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Size	Document Number	Rev
	STRAP (6/6)	1A
Date: Tuesday, November 18, 2014 Sheet 7 of 41		

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PROJECT : Y71
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Size B	Document Number Reserved	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 8 of 41		

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PROJECT : Y71
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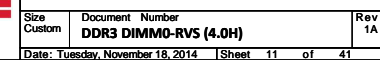
Size B	Document Number Reserved	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 9 of 41		

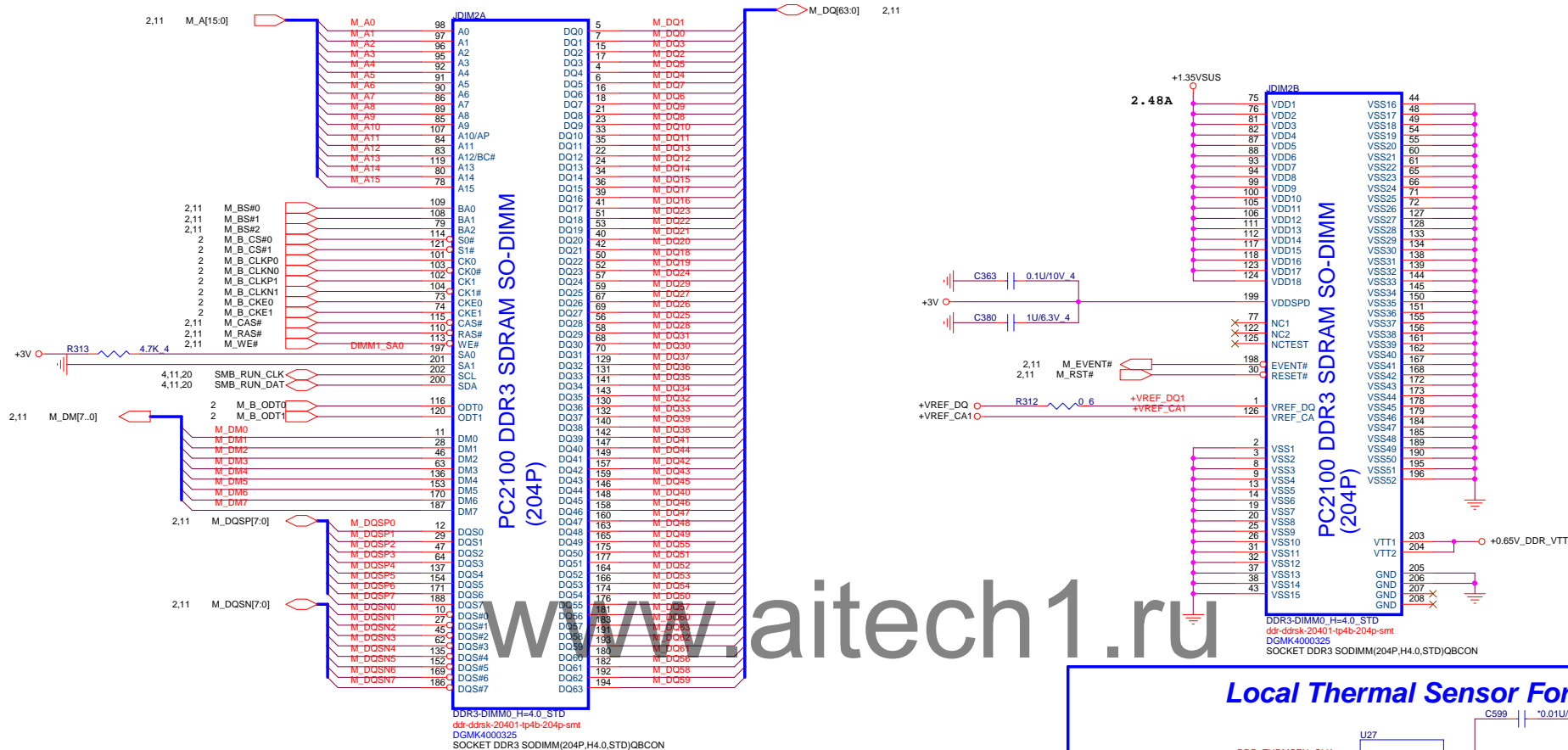
www.aitech1.ru



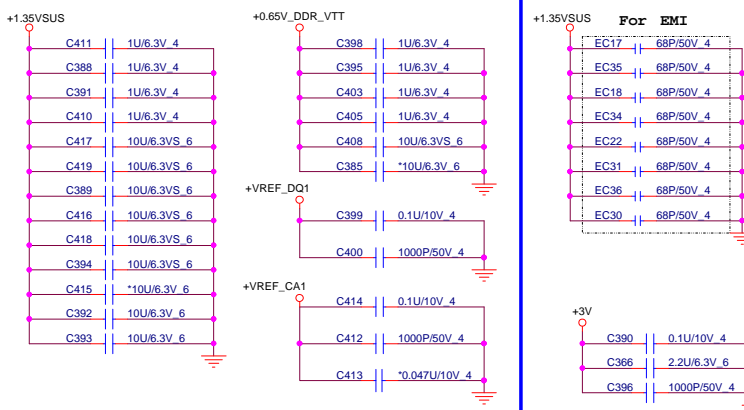
PROJECT : Y71
Quanta Computer Inc.

Size B	Document Number Reserved	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 10 of 41		

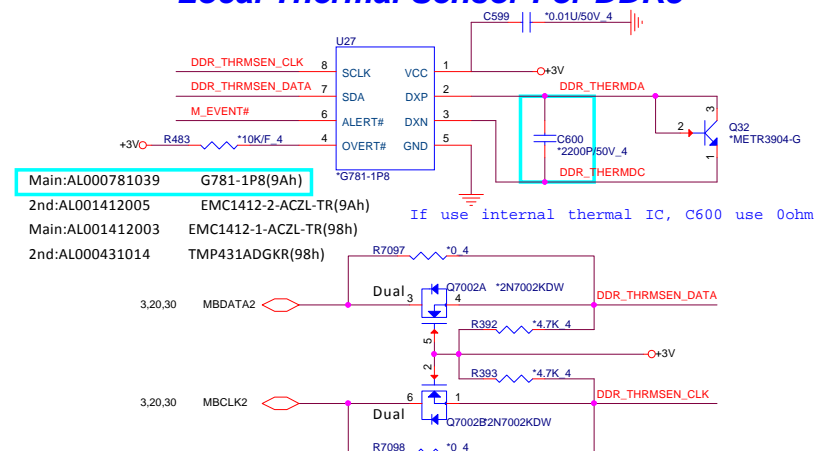




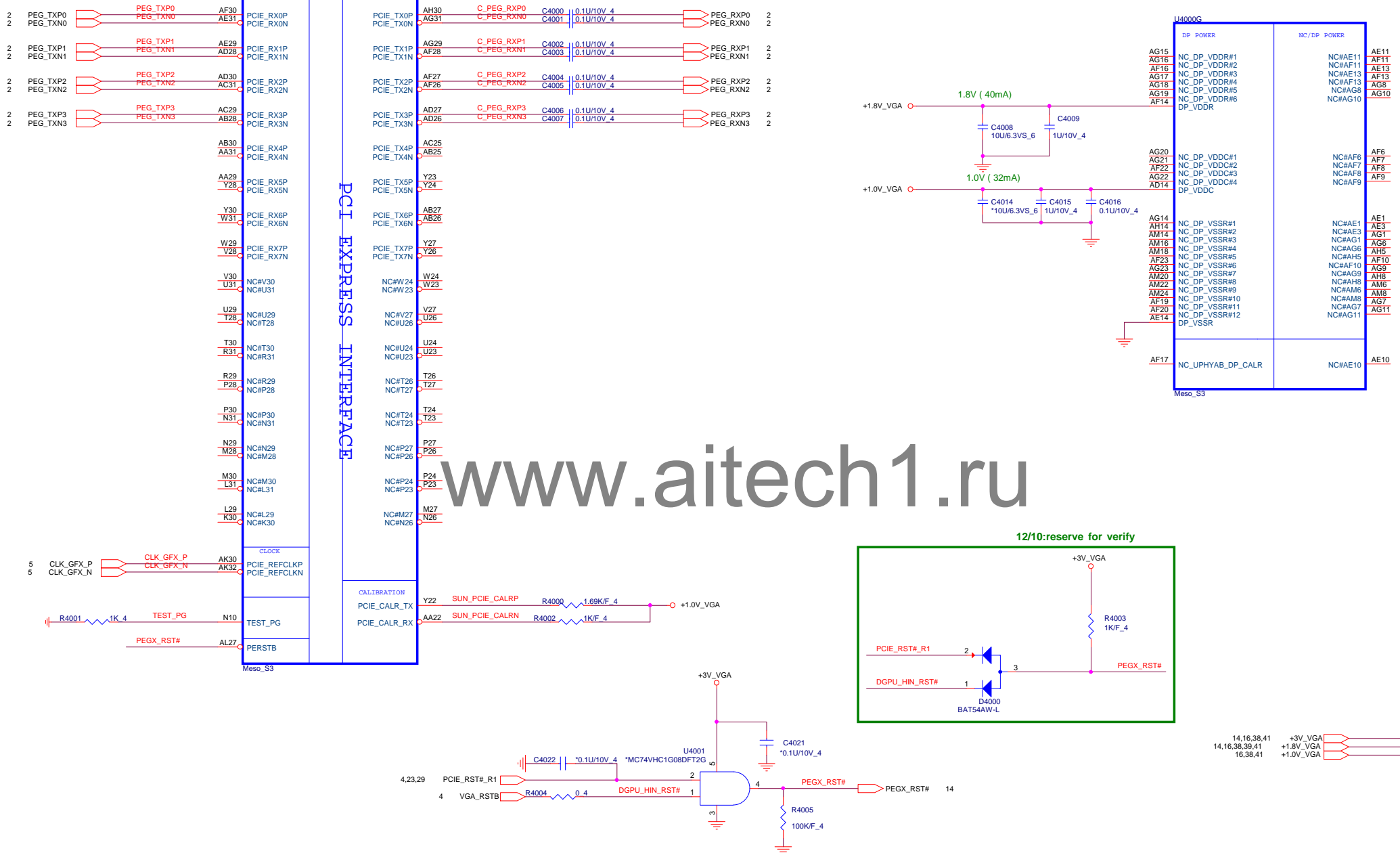
Place these Caps near So-Dimm1.

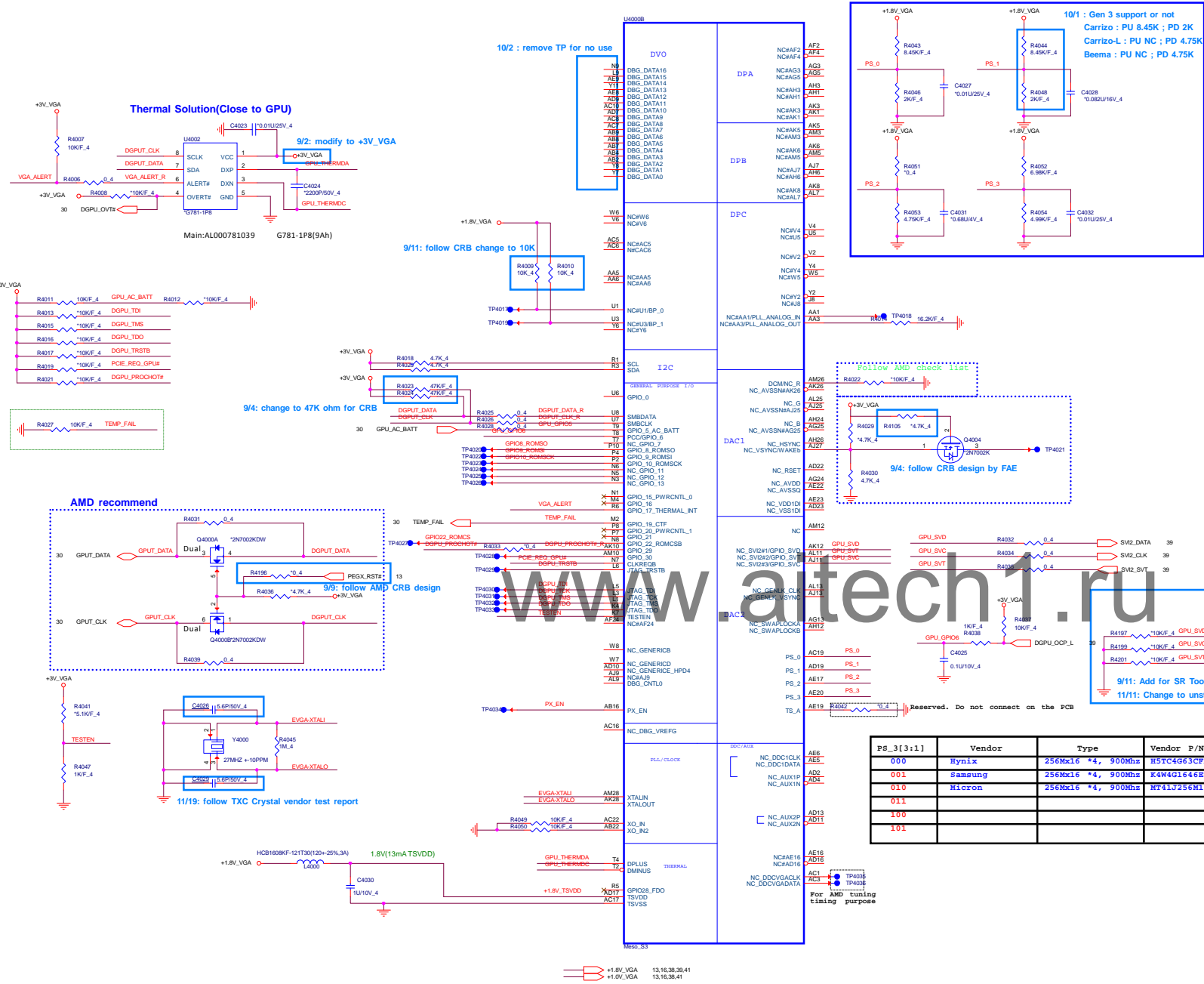


Local Thermal Sensor For DDR3



Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03





MLPS Implementation

- Connect GPU_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per table below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (pF)	Bin(3,4)	R _{pu} (Ohm)	R _{pd} (Ohm)	Bin(3,2,1)
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5630	101
		3400	10000	110
		4750	NC	111

Resistor Divider Lookup Table

C (pF)	Bin(3,4)	R _{pu} (Ohm)	R _{pd} (Ohm)	Bin(3,2,1)
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5630	101
		3400	10000	110
		4750	NC	111

MLPS BITs => BIT0

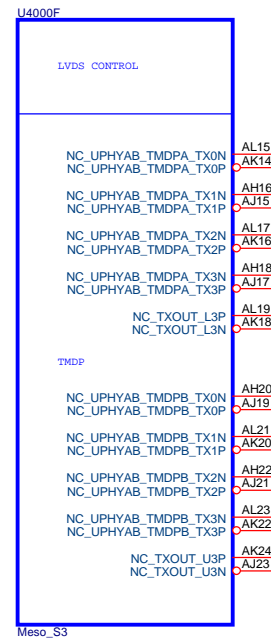
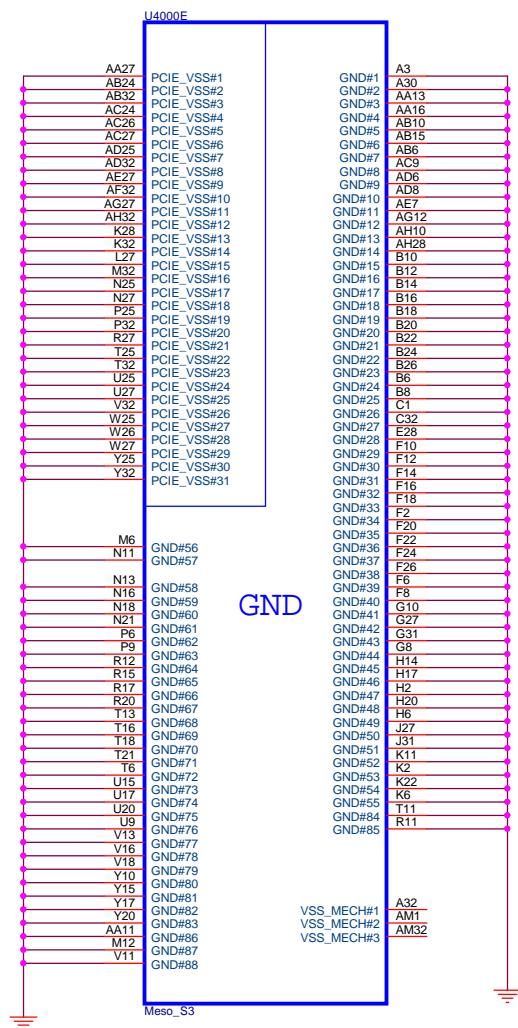
PS0 => 11001
PS1 => 11000
PS2 => 11000
PS3 => 11000

MLPS Circuit

PS_0, PS_1, PS_2, PS_3

MLPS Bit	Strap Name	Description	Recommended Settings
PS_011	ROM_CONFIG[0]	If STRAP BIOS_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
PS_012	ROM_CONFIG[1]	If STRAP BIOS_ROM_EN = 0, ROM_CONFIG[1] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 29)	
PS_013	ROM_CONFIG[2]		
PS_041	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_015	N/A	Reserved.	1
PS_111	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_112	STRAP_BIF_CLK_PM_EN	Deformatter whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_113	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_114	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_115	STRAP_TX_DEEMPH_EN	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_211	N/A	Reserved.	0
PS_212	N/A	Reserved.	0
PS_213	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_214	N/A	Reserved.	1
PS_215	N/A	Reserved	1
PS_311	BOARD_CONFIG[0]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_312	BOARD_CONFIG[1]		
PS_313	BOARD_CONFIG[2]		
PS_314	N/A	Reserved.	1
PS_315	N/A	Reserved.	1

PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Hynix	256Mx16 *4, 900Mhz	H5TC4G63CFR-N0C	NC	4.75K
001	Samsung	256Mx16 *4, 900Mhz	K4W4G1646E-BC1A	8.45K	2K
010	Micron	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	4.53K	2K
011					
100					
101					



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

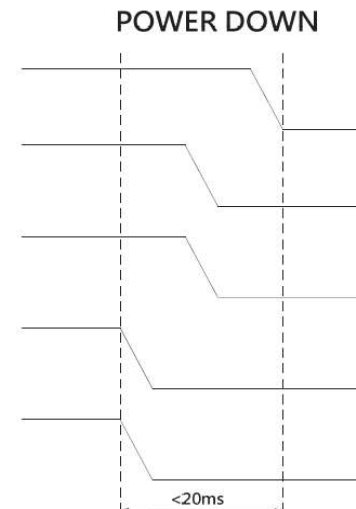
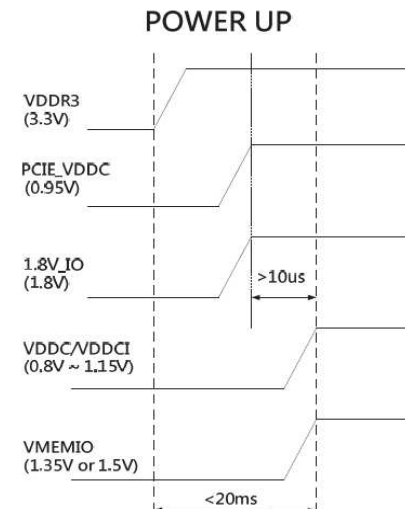
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	x
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

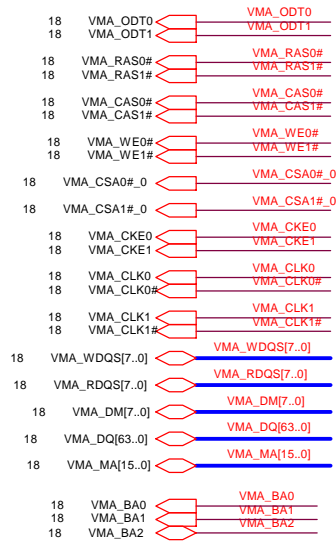


NB5/RD3

PROJECT : X22
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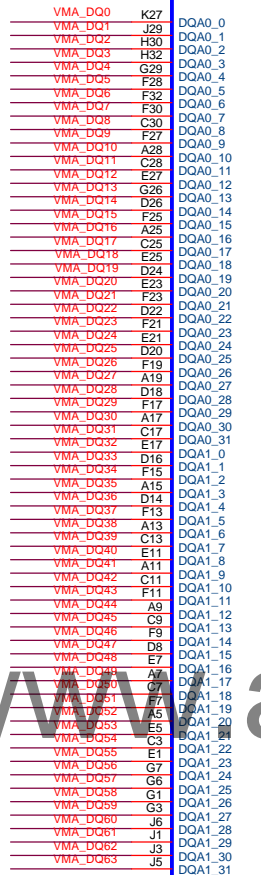
Size	Document Number	Rev
	MESO_S3_GND/LVDS/Strap	1A
Date:	Tuesday, November 18, 2014	Sheet 15 of 43



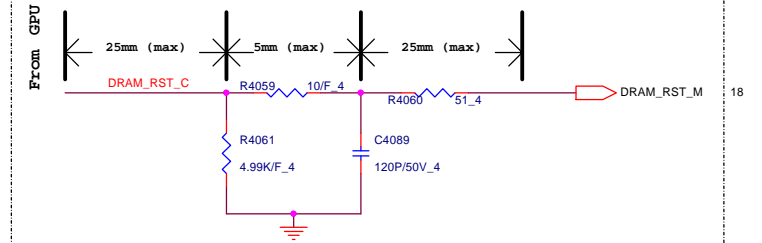
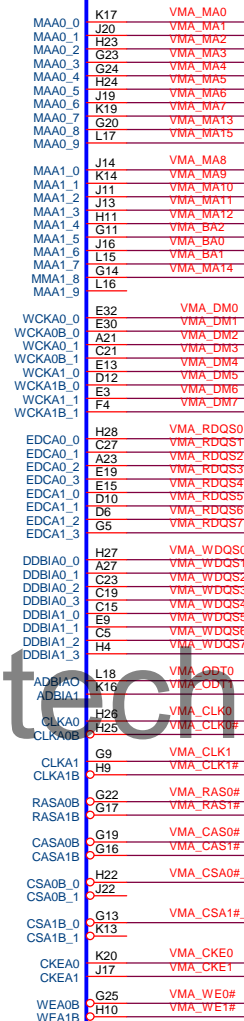


support 1Gbit
VRAM (64M x 16)

U4000C

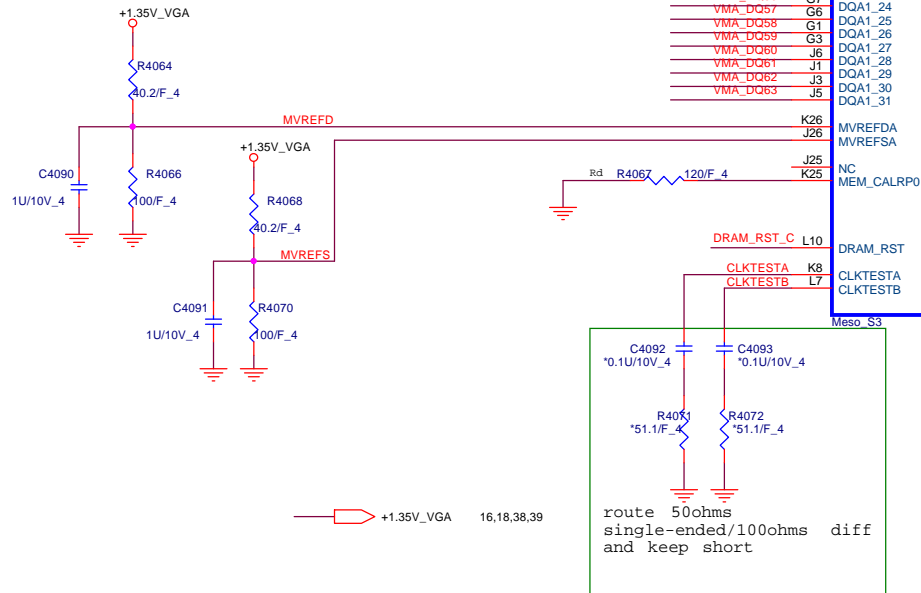


MEMORY INTERFACE



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.



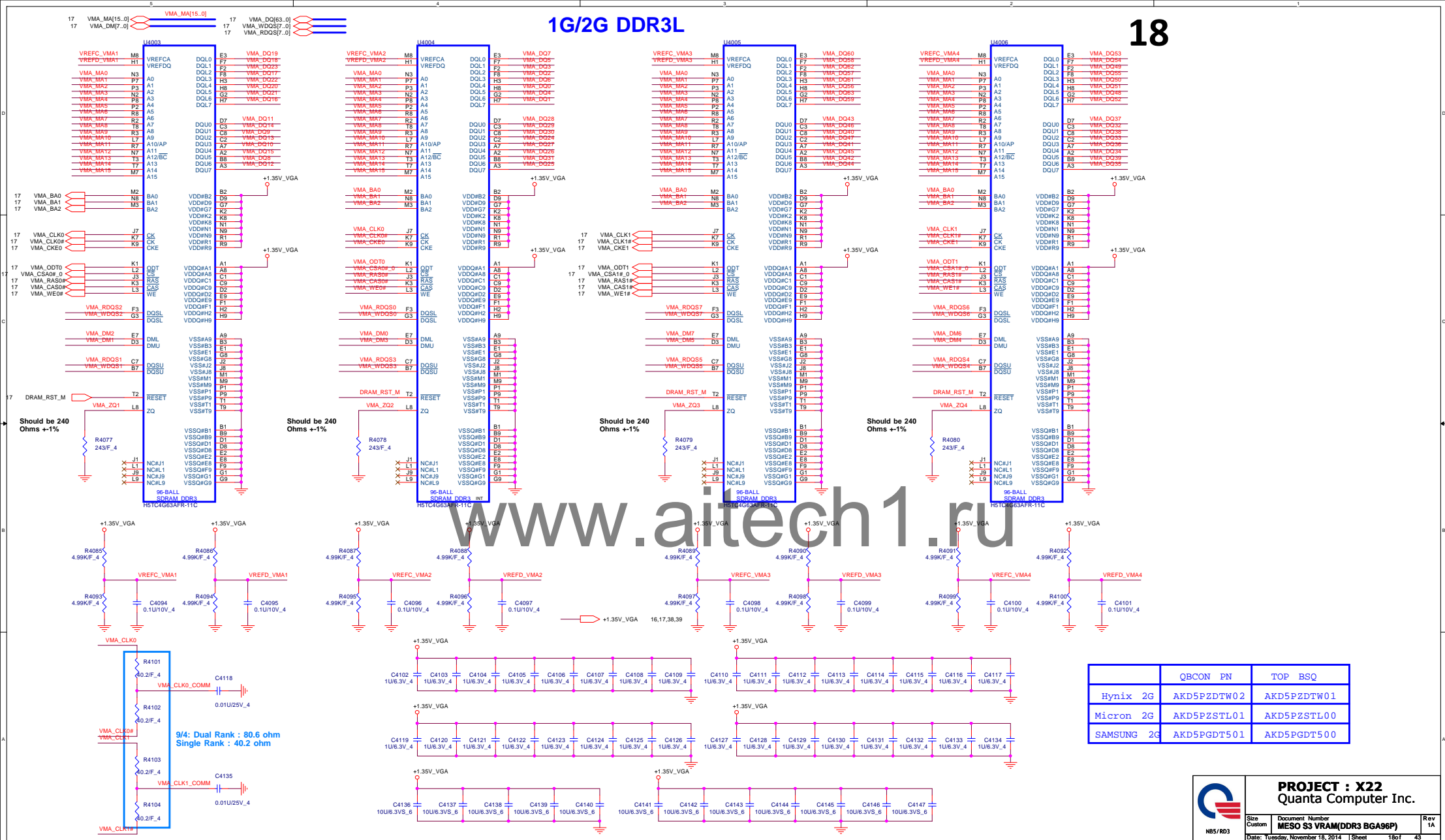
NB5/RD3

PROJECT : X22
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Size	Document Number	Rev
	MESO_S3_MEM_Interface	1A
Date:	Tuesday, November 18, 2014	Sheet 17 of 43

1G/2G DDR3L

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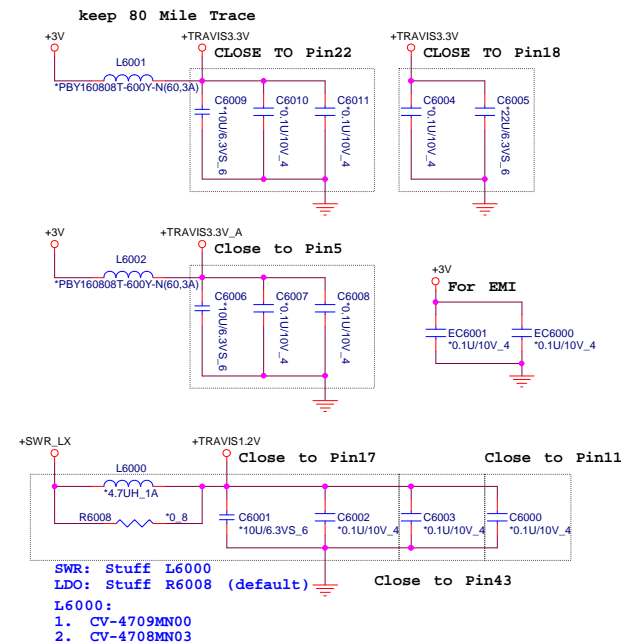
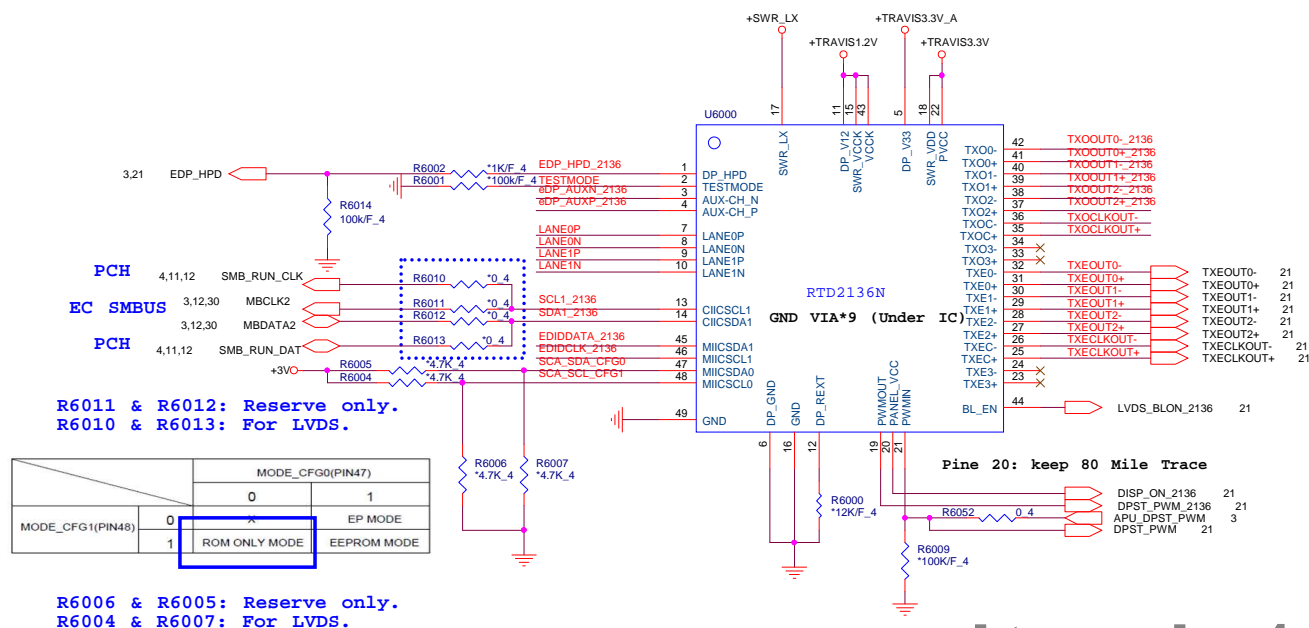


NBS/RD3

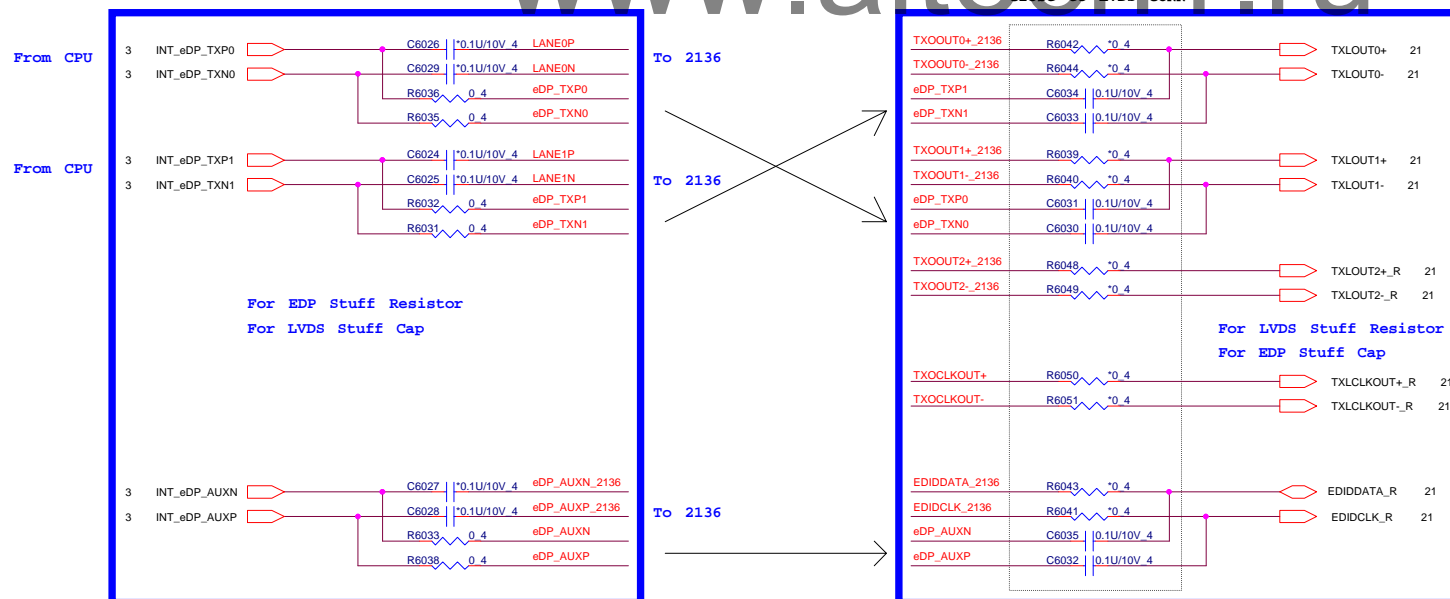
PROJECT : X22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MESO S3 VRAM(DDR3 BGA96P)	1A
Date: Tuesday, November 18, 2014 Sheet 1801 43		

Pine 15/17: keep 20 Mile Trace
Pine 18: keep 80 Mile Trace



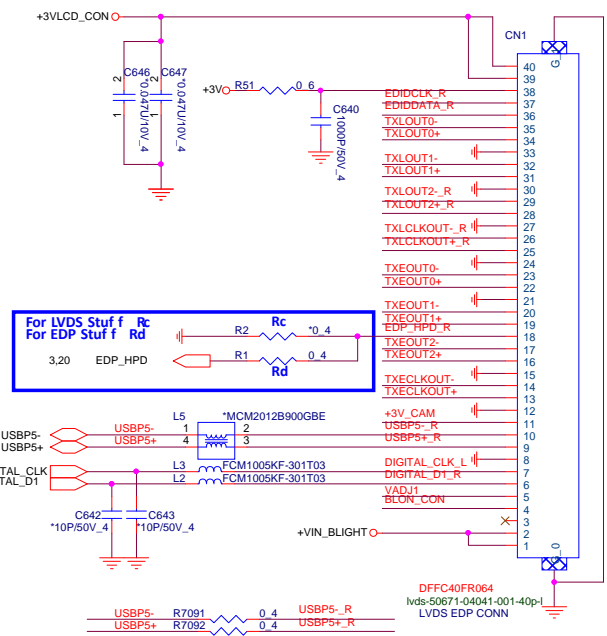
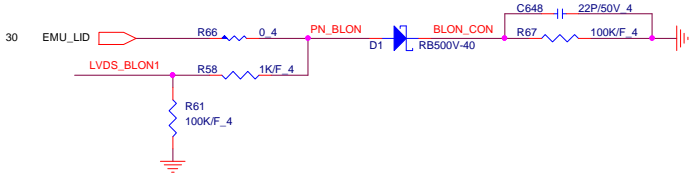
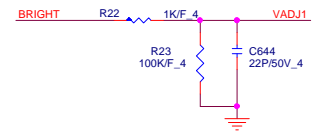
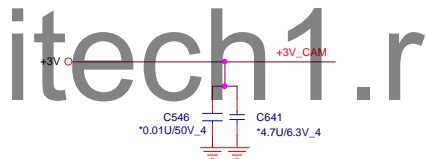
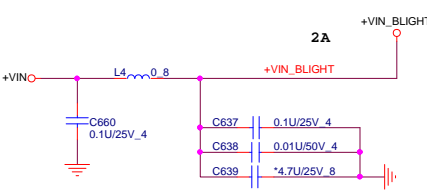
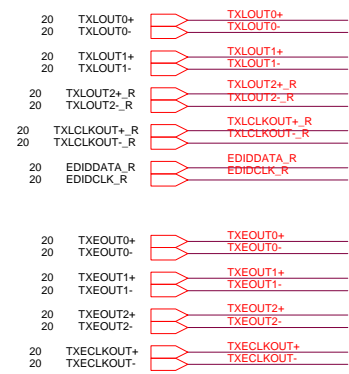
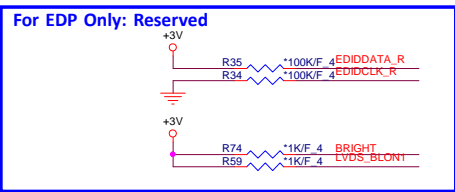
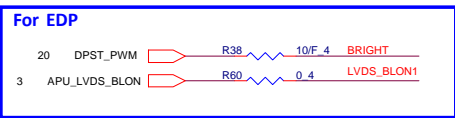
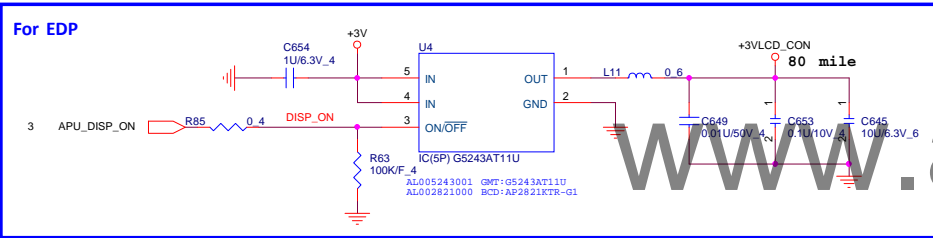
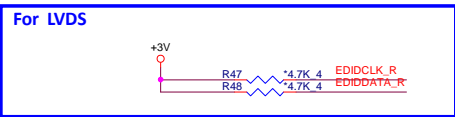
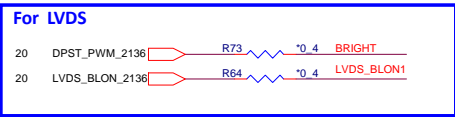
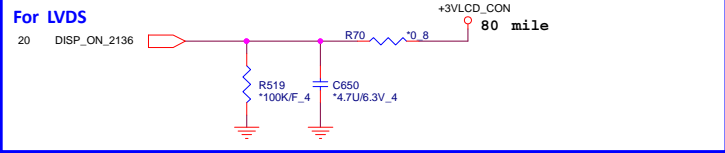
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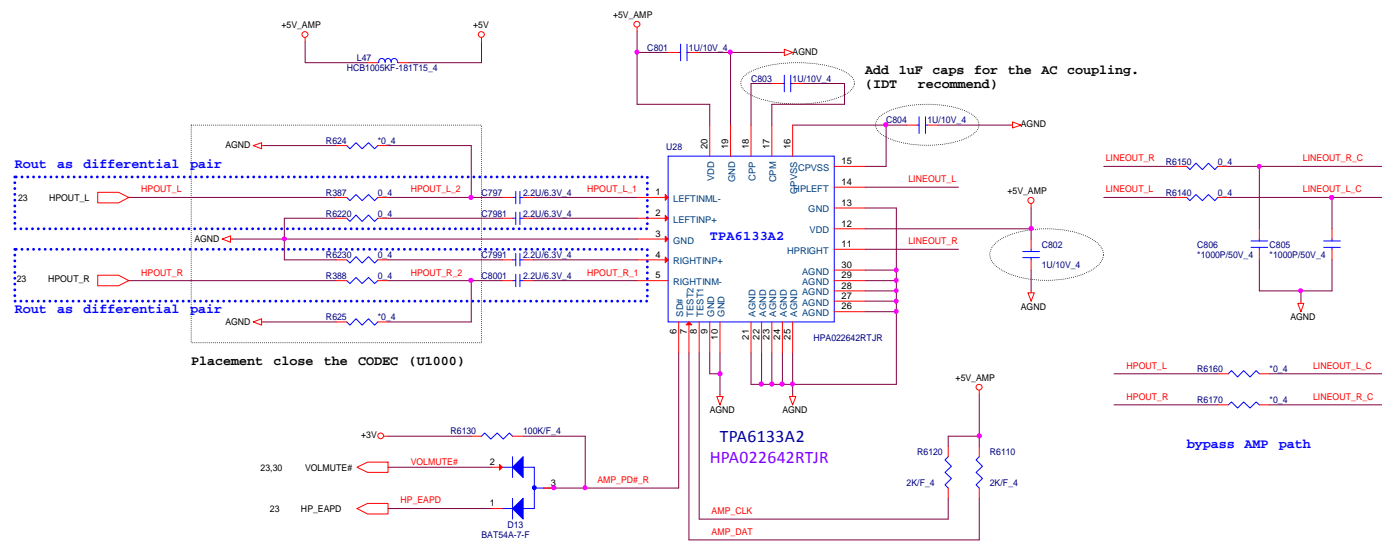


Note.
14" & 15" only eDP panel.
17" have both LVDS & eDP panel.

LVDS CONN.

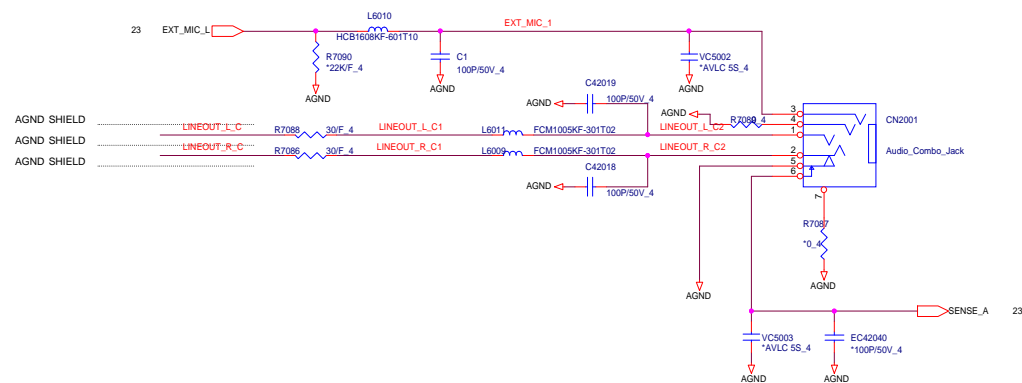
Note.
14" & 15" only eDP panel.
17" have both LVDS & eDP panel.



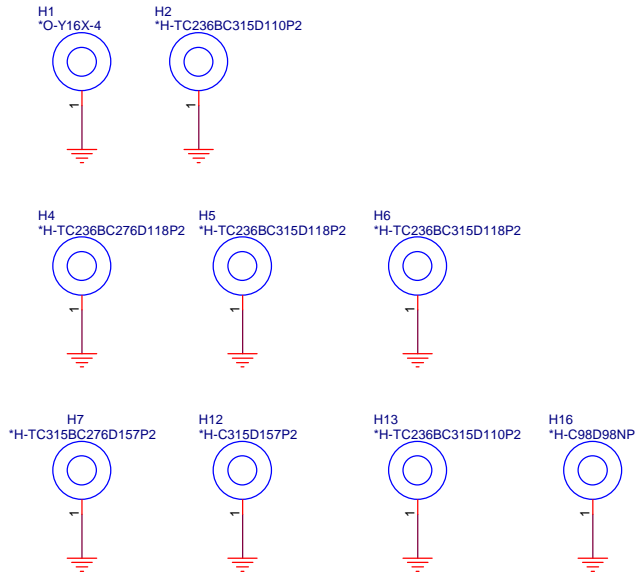


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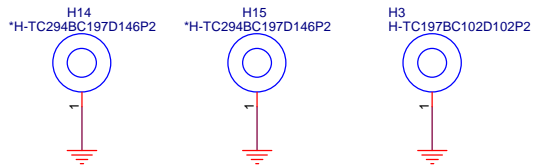
Audio Combo



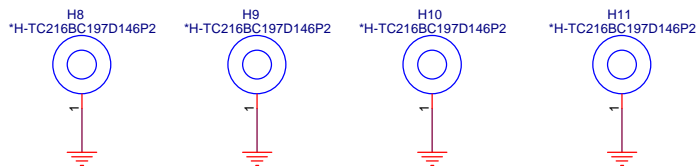
Holes



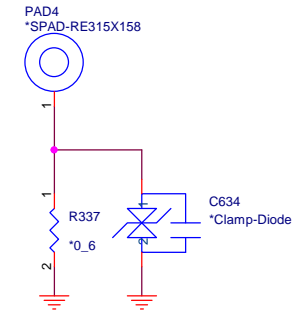
GPU HOLES



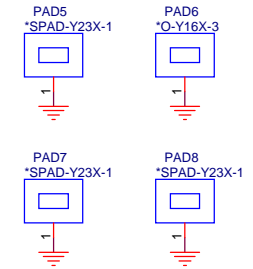
APU HOLES



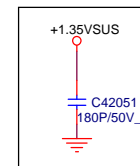
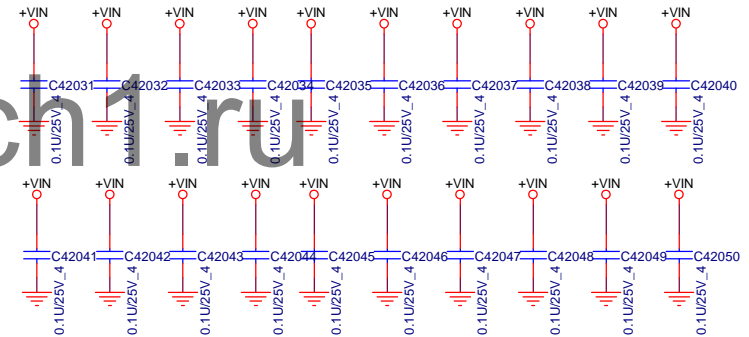
Metal ESD



EMI



Place on +VIN path



11/17 EMI request



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Quanta Computer Inc.

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	Holes / EMI	1A
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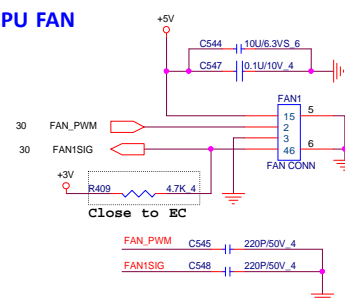
NB5/RD3

PROJECT : Y2x
Quanta Computer Inc.

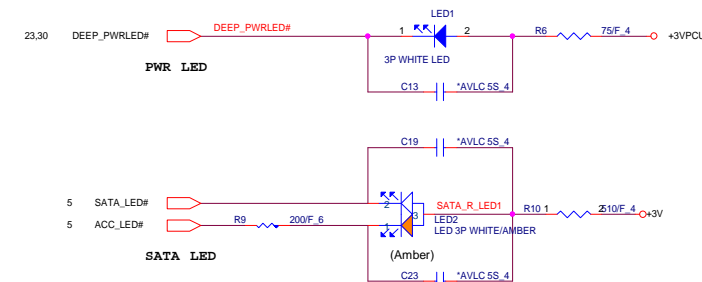
Size B	Document Number Reserved	Rev 1A
Date: Tuesday, November 18, 2014		
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Power But t on Connect or (Momet o DB)

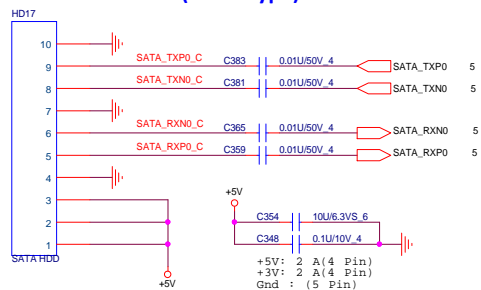
CPU FAN



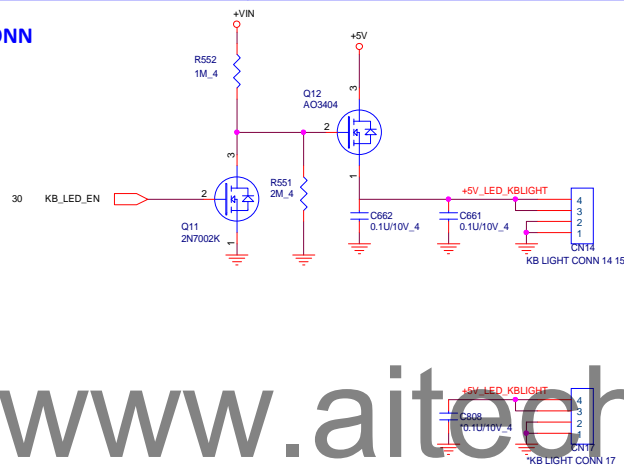
LED



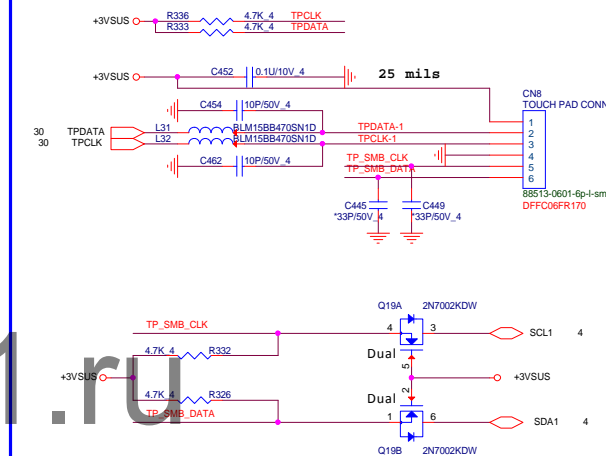
SATA HDD CONN (Cable type)



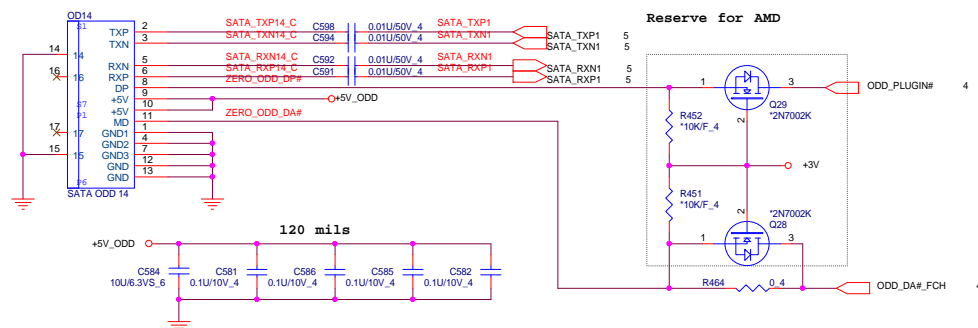
KB LIGHT CONN



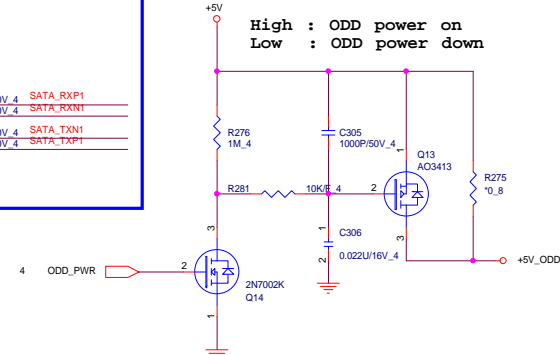
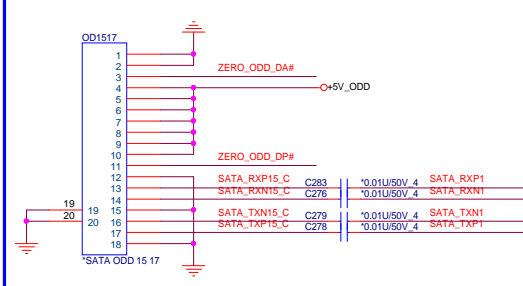
Touch Pad



14" SATA ODD CONN

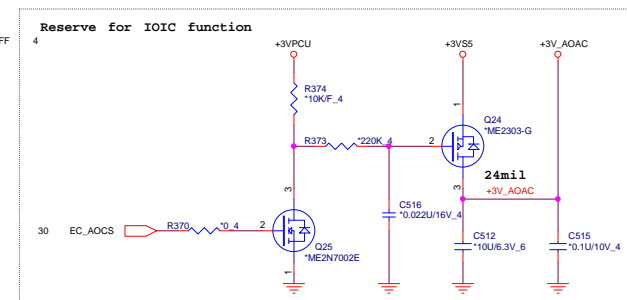
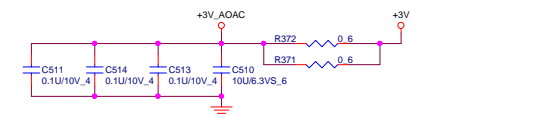
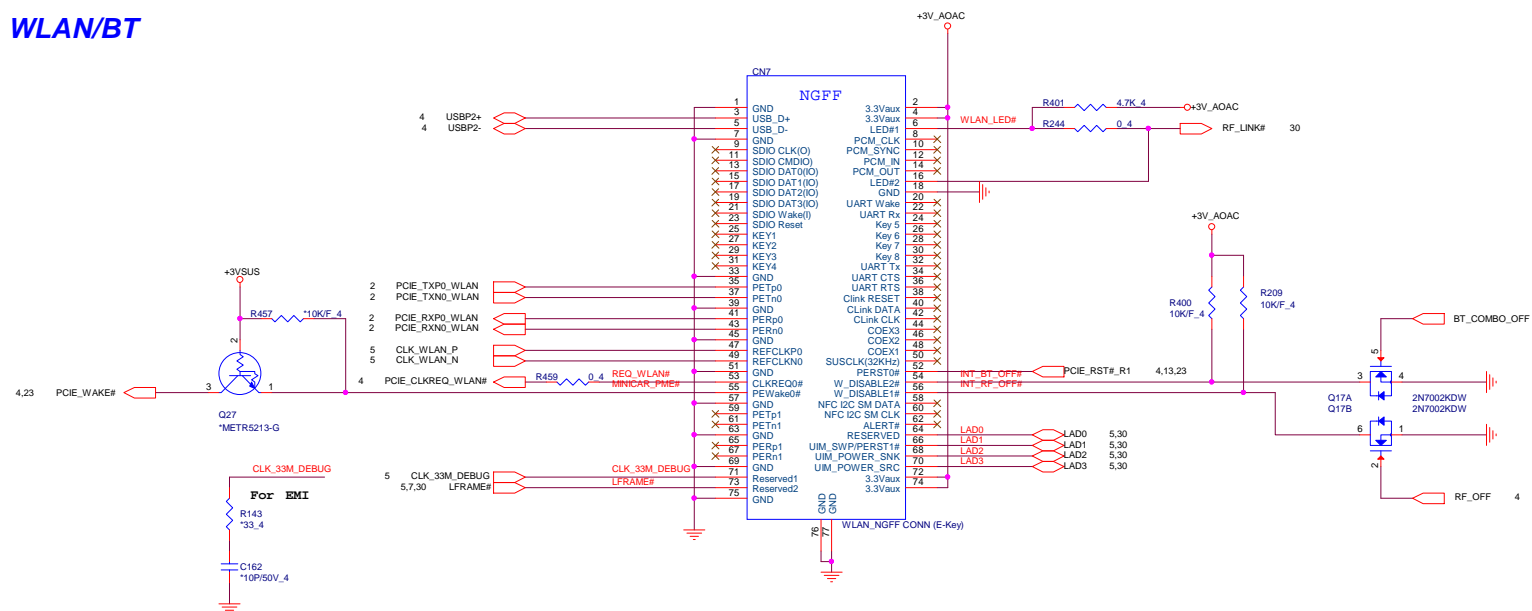


15" & 17" SATA ODD CONN

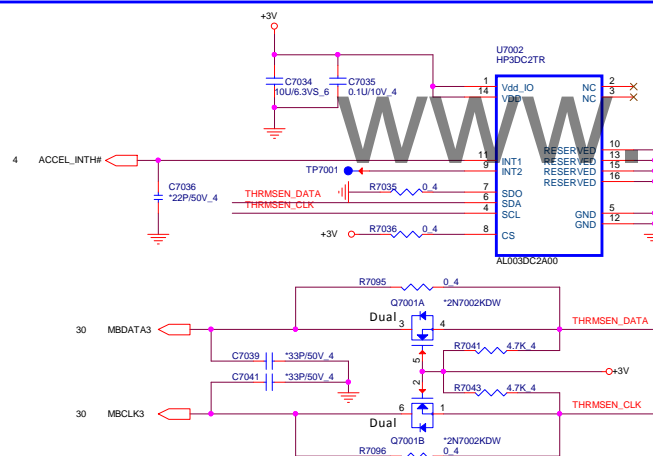


PROJECT : Y2x
Quanta Computer Inc.

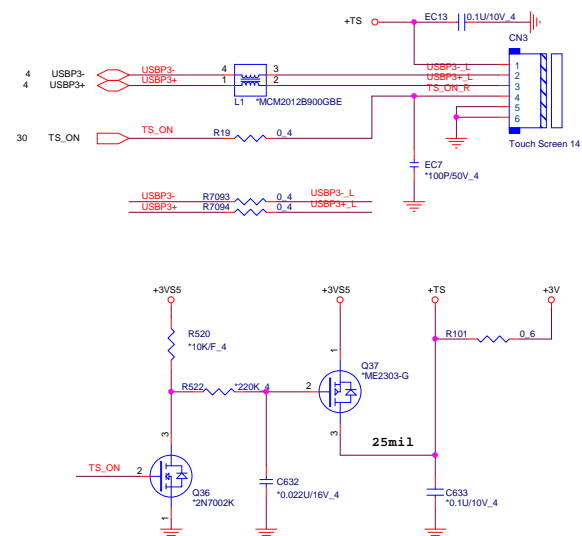
Size	Document Number	Rev
Custom	HDD/ODD/TP/FAN/LID/LED	1A
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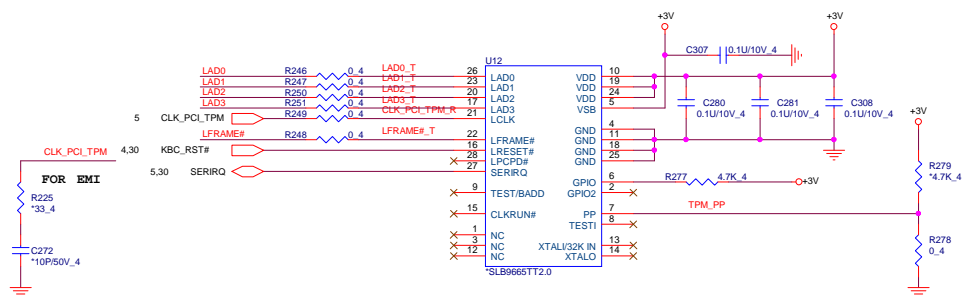
Accelerometer Sensor

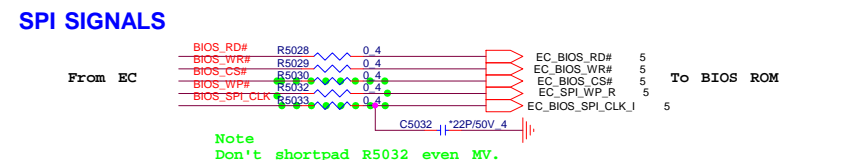
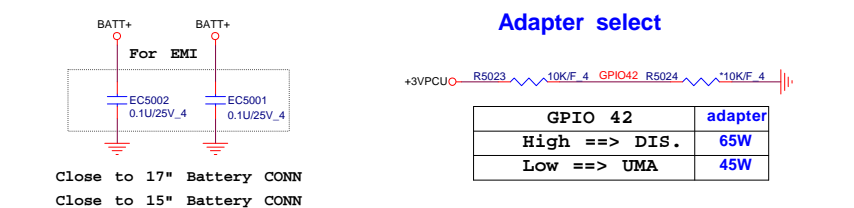
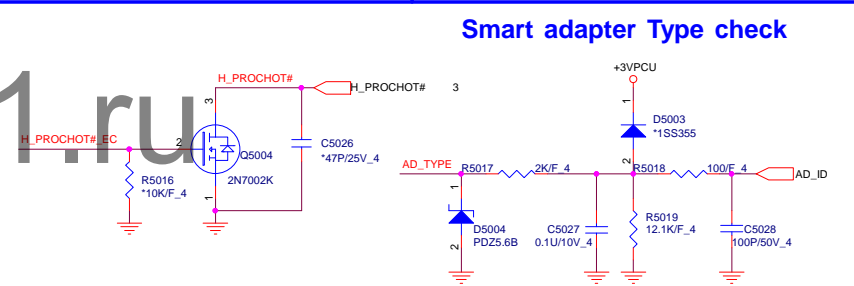
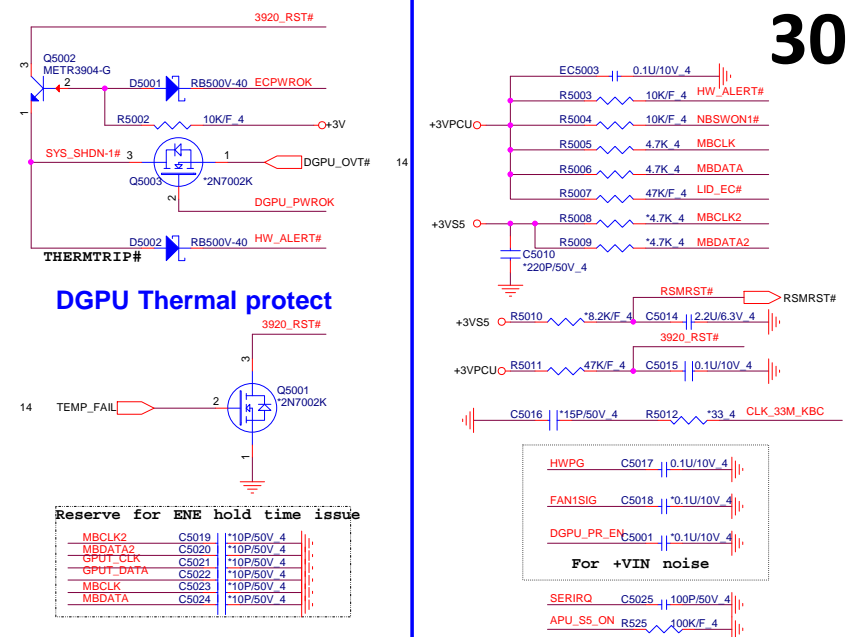
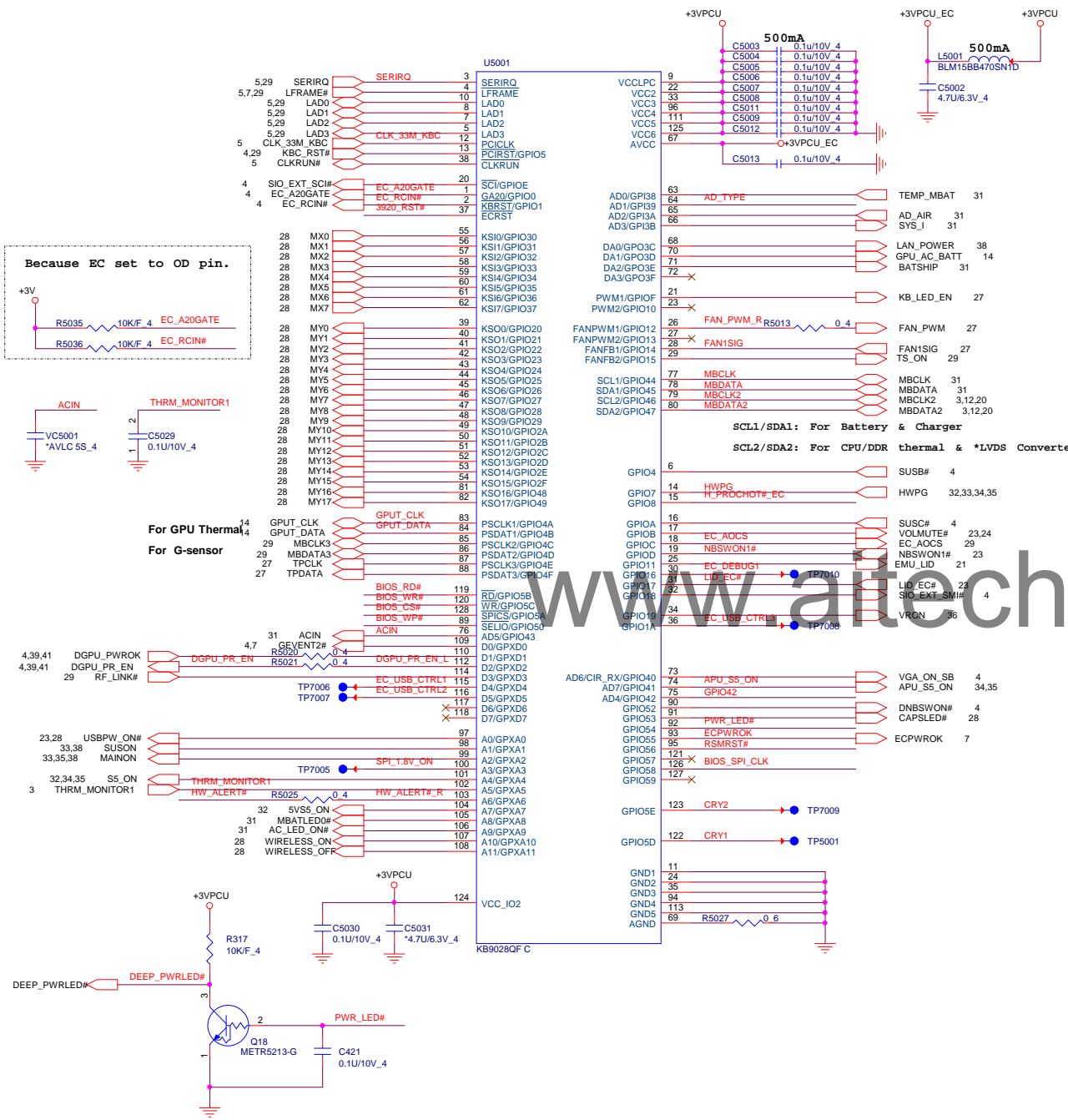



Touch screen

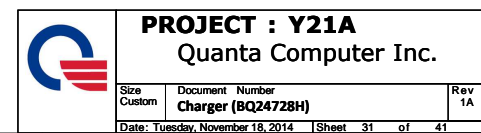


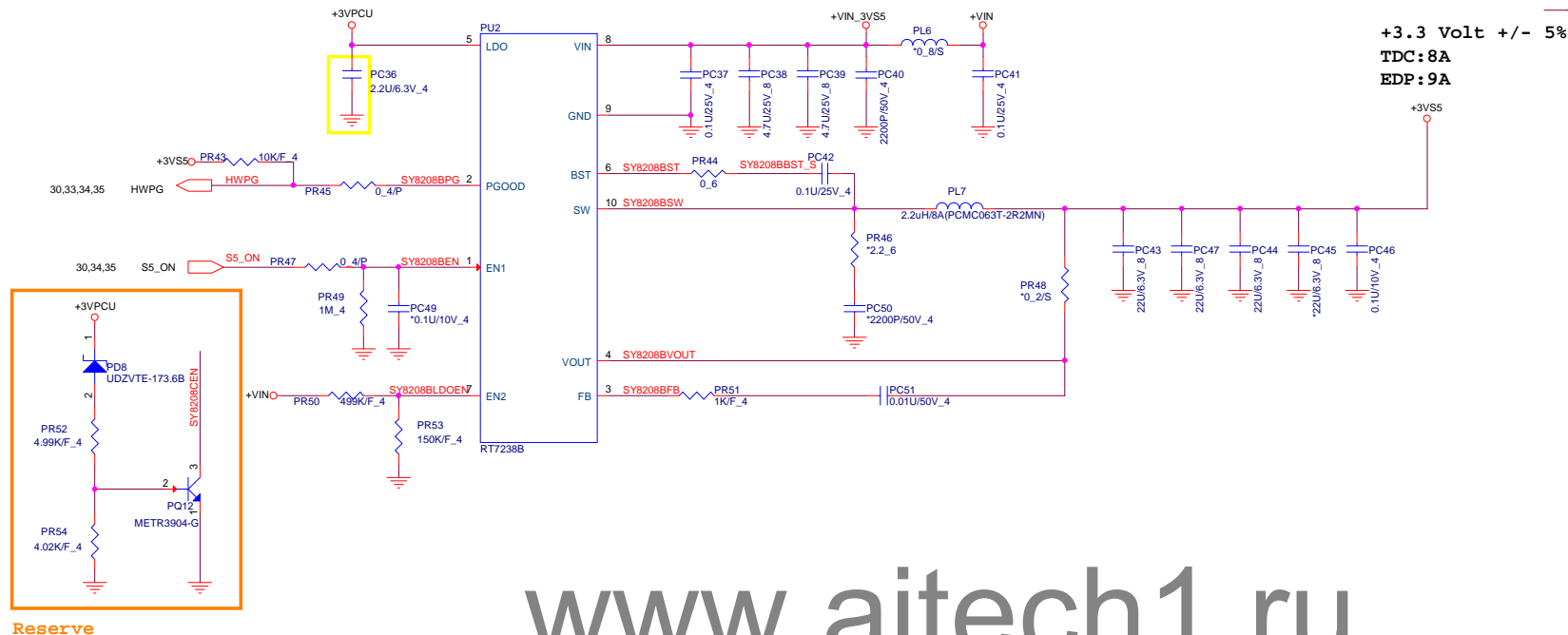
TPM (2.0)





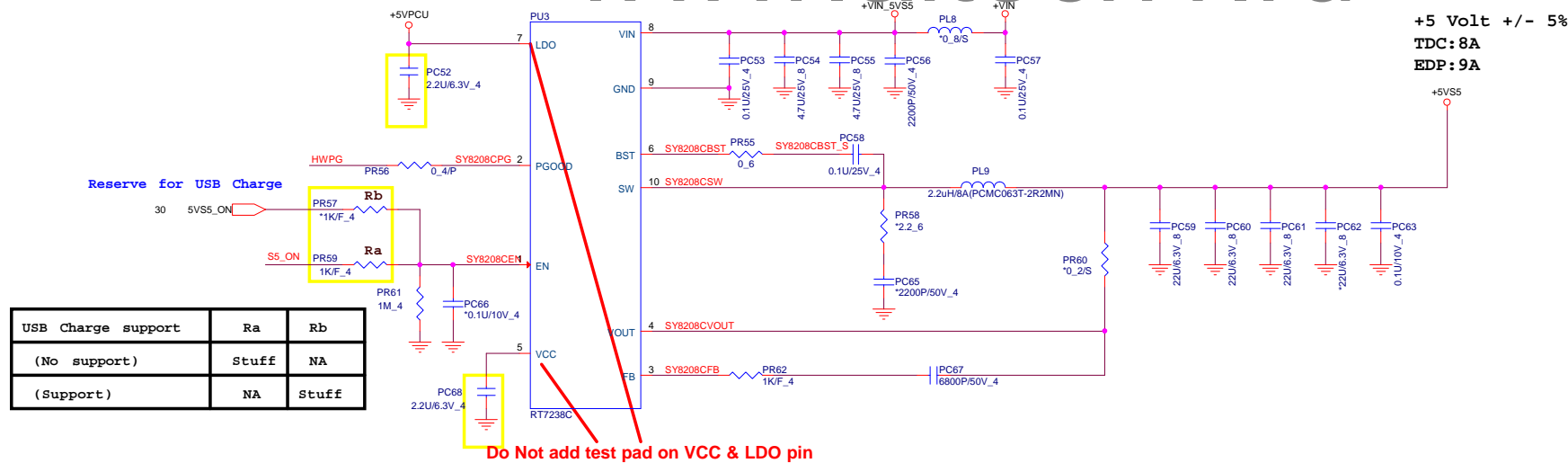
 NB5/RD3	PROJECT : Y2x Quanta Computer Inc.		
	Size Custom	Document Number EC KB9028QF	Revision 1A
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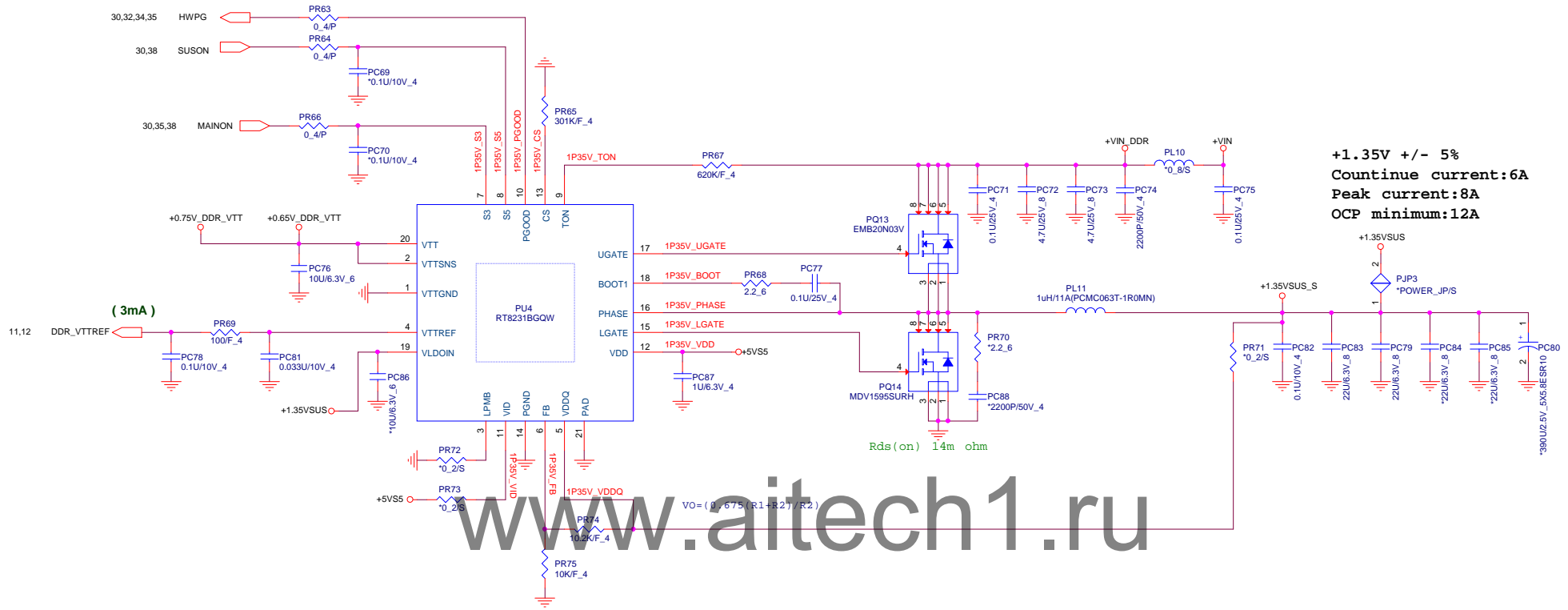




Reserve

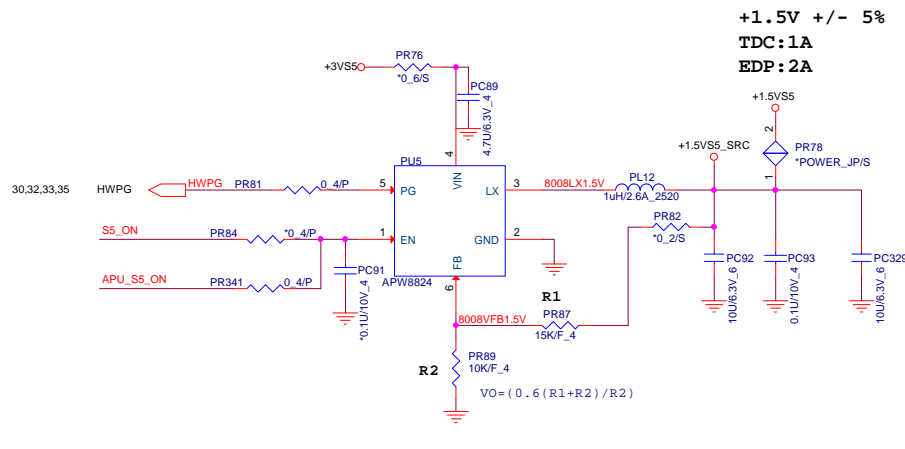
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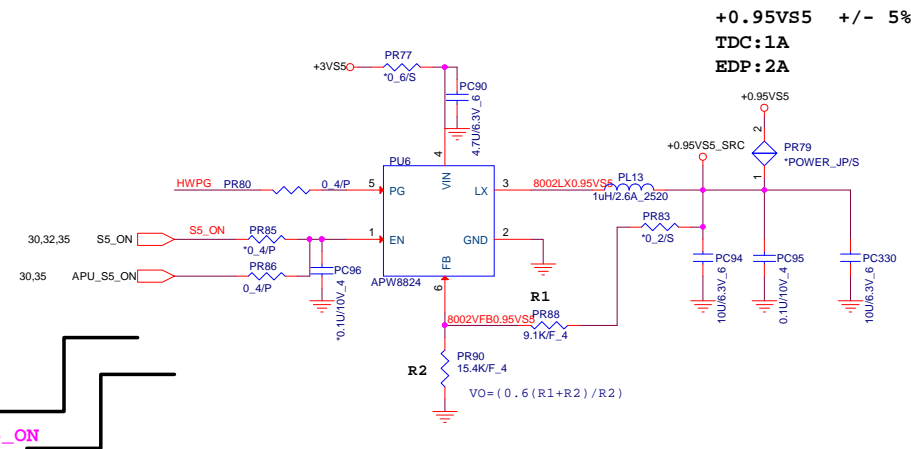
+1.35V +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

+1.35VSUS 2.6,11,12,25

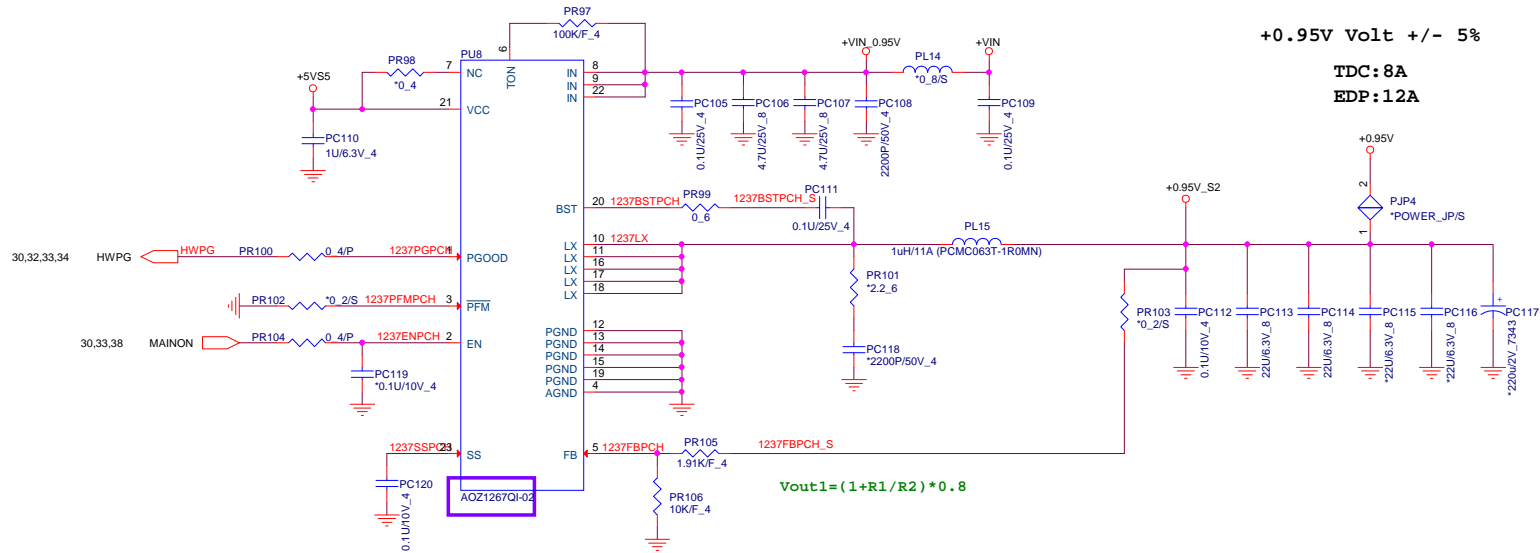


S5_ON

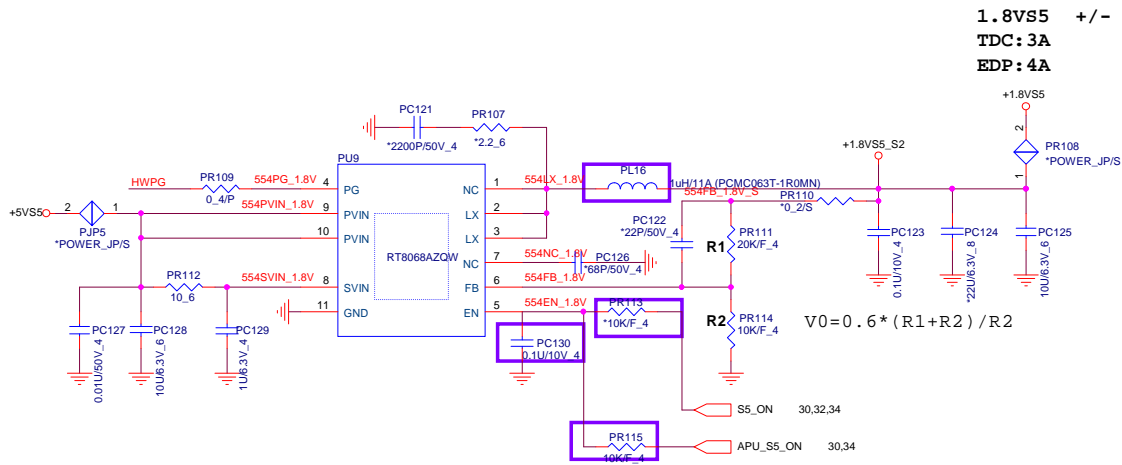
APU_S5_ON

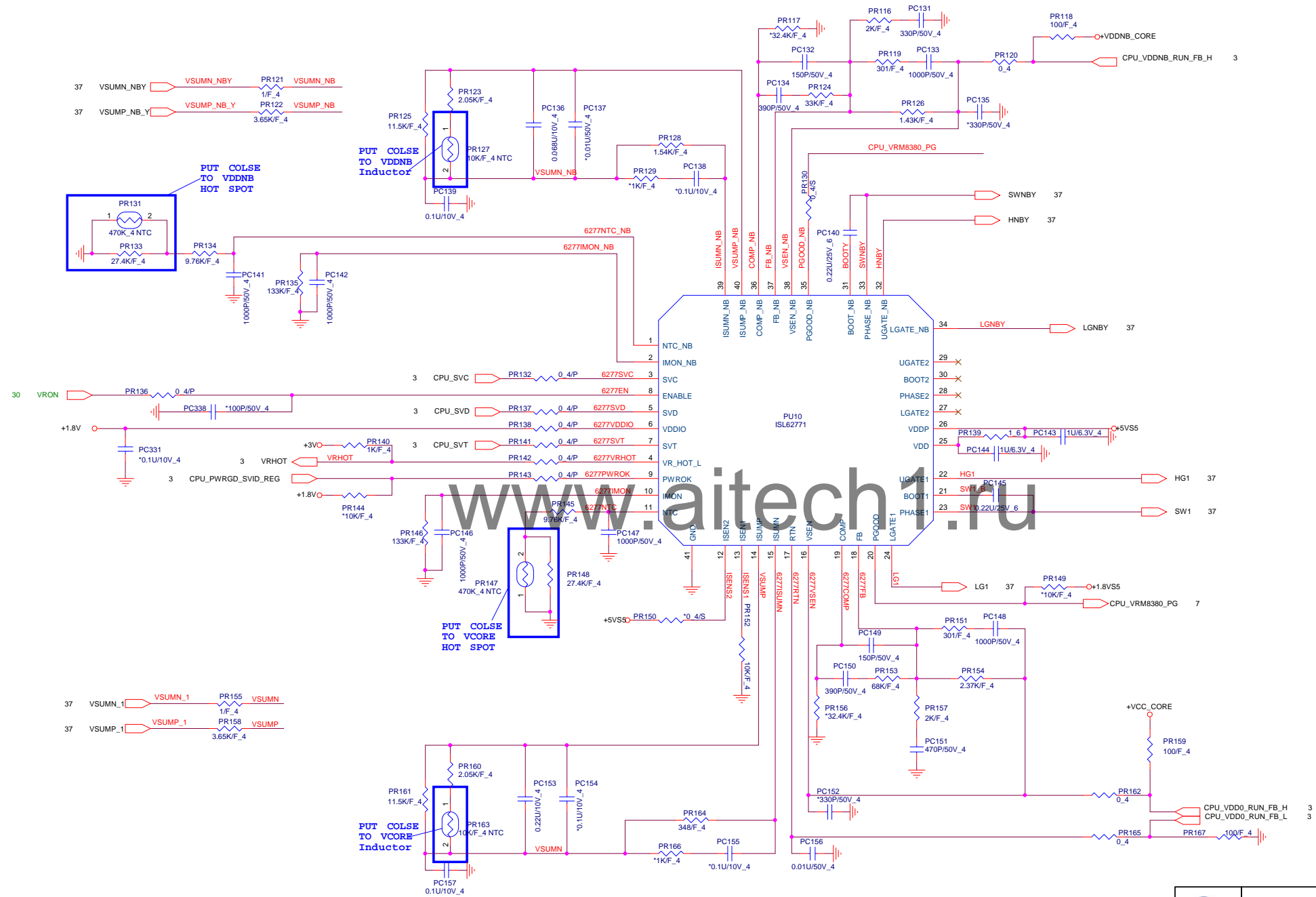


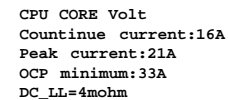
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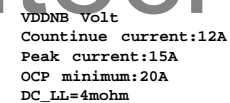
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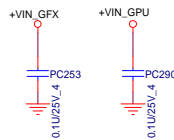
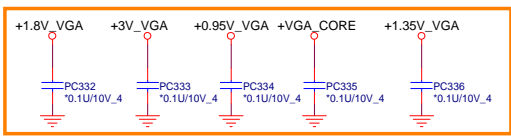




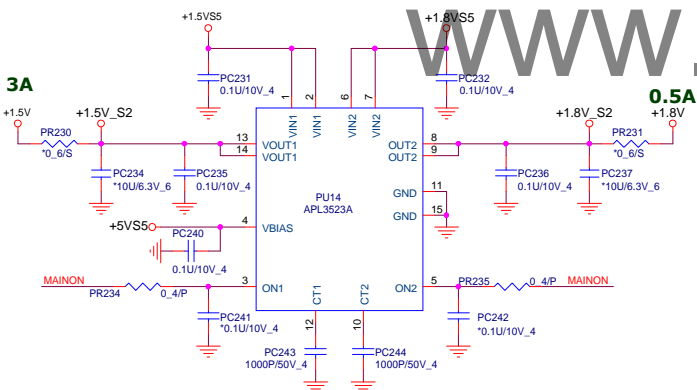
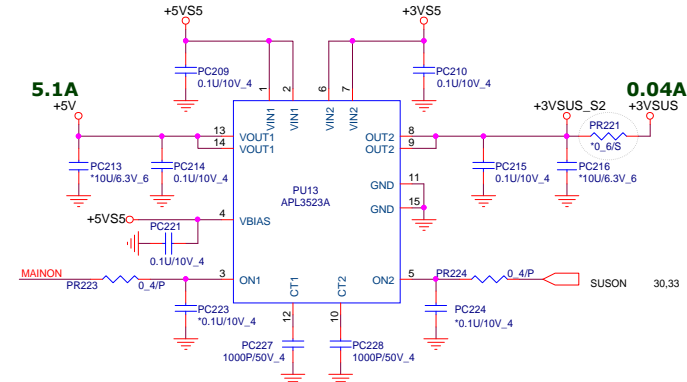
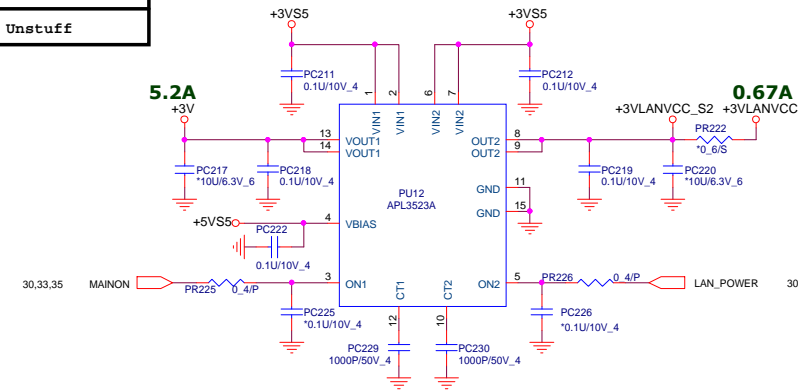


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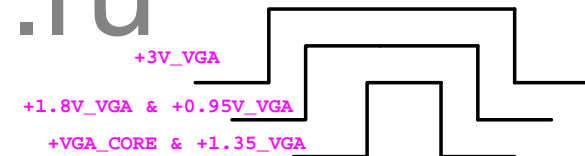
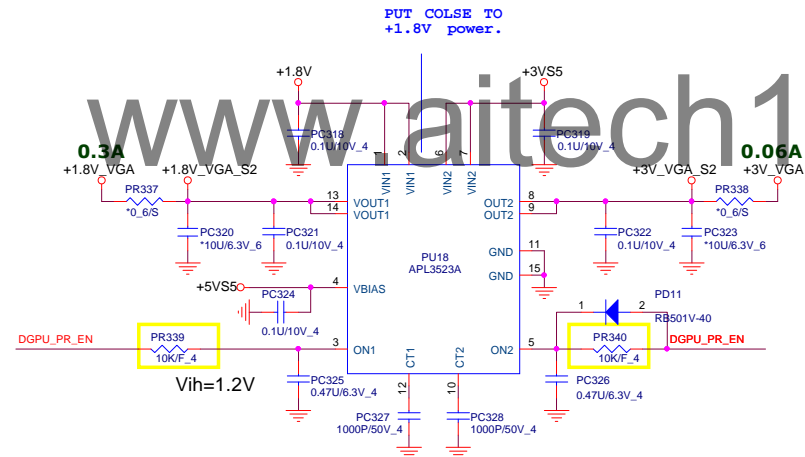
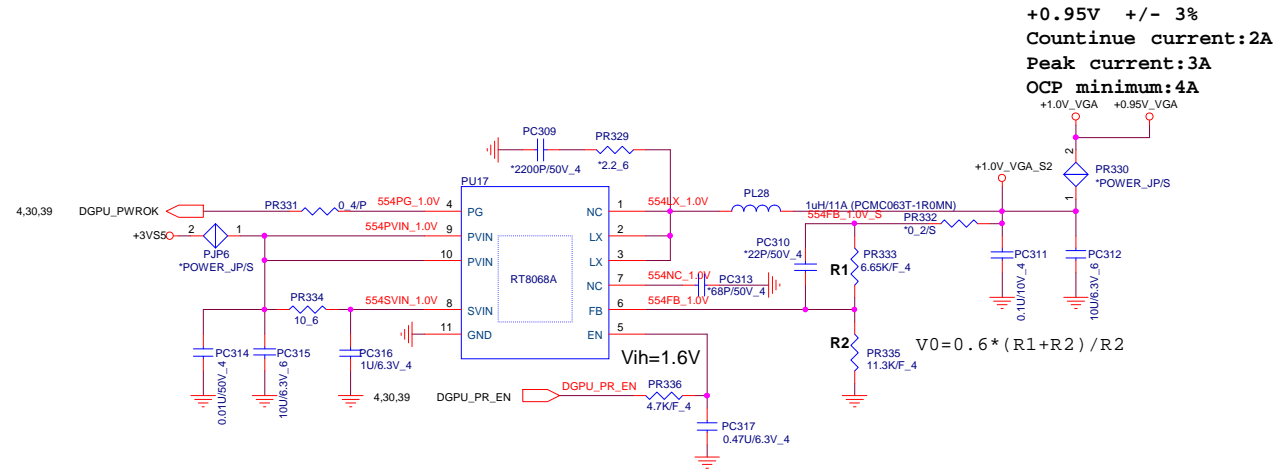




UMA only	Stuff
discrete	Unstuff



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+3V_VGA 13,14,16,38
+1.0V_VGA 13,16,38
+1.8V_VGA 13,14,16,38,39